PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN POWER INVERTERS AND CONVERTERS, VEHICLES CONTAINING THE SAME, AND COMPONENTS THEREOF**	**Inv. No. 337-TA-1267**

FINAL INITIAL DETERMINATION ON VIOLATION OF SECTION 337

Administrative Law Judge Monica Bhattacharyya

(August 12, 2022)

Appearances:

For Complainant Arigna Technology Limited:

Matthew R. Berry, Rachel S. Black, Andres Healy, John Schiltz, Nicholas Crown, and Danielle Nicholson of Susman Godfrey LLP in Seattle, WA; Oleg Elkhunovich of Susman Godfrey LLP in Los Angeles, CA; Bryce T. Barcelo and Tom DelRosario of Susman Godfrey LLP in Houston, TX; Reza Mirzaie and Brett Cooper of Russ August & Kabat in Los Angeles, CA; and Matthew D. Aichele and Jonathan Link of Russ August & Kabat in Washington, DC.

For Respondents Volkswagen AG, Volkswagen Group of America, Inc., Audi AG, Audi of America, LLC, Bentley Motors Limited, Bentley Motors, Inc., Automobili Lamborghini S.p.A., and Automobili Lamborghini America, LLC:

Mareesa A. Frederick, J. Preston Long, Gerald F. Ivey, Amy Fulton, and Matthew R. Ritter of Finnegan, Henderson, Farabow, Garrett & Dunner LLP in Washington, DC; and John M. Mulcahy, Elliott Cook, Yi Yu, and Dan Jordan of Finnegan, Henderson, Farabow, Garett & Dunner LLP in Reston, VA.

For Respondents Bayerische Motoren Worke AG and BMW of North America, LLC:

Smith R. Brittingham, R. Benjamin Cassady, Michael J. Aragon, Matthew C. Berntsen, Michael J. McLaughlin, and Lionel M. Lavenue of Finnegan, Henderson, Farabow, Garrett & Dunner LLP in Washington, DC; Robert Fernandes and Sneha Nyshadham of Finnegan, Henderson, Farabow, Garrett & Dunner in Palo Alto, CA; and Max Mauldin of Finnegan, Henderson, Farabow, Garrett & Dunner in Atlanta, GA

For Respondent General Motors LLC:

Michael J. McKeon, Christian A. Chu, and Jared Hartzman of Fish & Richardson in Washington, DC; Tim Rawson of Fish & Richardson in San Diego, CA; Leeron Kalay of Fish & Richardson in Redwood City, CA; and Joe Herriges of Fish & Richardson in Minneapolis, MN.

For Respondents Daimler AG and Mercedes-Benz USA, LLC:

Celine J. Crowson, Joseph J. Raffetto, Scott Hughes, Anna Kurian Shaw, Ryan J. Stephenson, Nicholas W. Rotz, Yi Sally Zhang, Michael Kosuge, and Eric Wang of Hogan Lovells US LLP in Washington, DC; Lisa Dong of Hogan Lovells US LLP in Denver, CO; and Helen Y. Trac of Hogan Lovells US LLP in San Francisco, CA.

For the Office of Unfair Import Investigations:

W. Peter Guarnieri and David O. Lloyd of the U.S. International Trade Commission in Washington, DC.

Pursuant to the Notice of Investigation (EDIS Doc. ID 745316), 86 Fed. Reg. 34042-43 (Jun. 28, 2021), and Commission Rule 210.42, this is the administrative law judge's final initial determination in the matter of *Certain Power Inverters and Converters, Vehicles Containing the Same, and Components Thereof,* Commission Investigation No. 337-TA-1267. 19 C.F.R. § 210.42(a)(1)(i).

For the reasons discussed herein, it is the undersigned's final initial determination that there has been no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, and/or the sale within the United States after importation of certain power inverters and converters used in automobiles, components thereof, and automobiles containing those power inverters or converters by reason of infringement of claims of U.S. Patent No. 8,247,867 or U.S. Patent No. 8,289,082.

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The following abbreviations may be used in this Initial Determination:

Tr.	Hearing Transcript
Dep. Tr.	Deposition Transcript
JX	Joint Exhibit
CX	Complainants' exhibit
CPX	Complainants' physical exhibit
CDX	Complainants' demonstrative exhibit
RX	Respondents' exhibit
RPX	Respondents' physical exhibit
RDX	Respondents' demonstrative exhibit
CPHB	Complainants' pre-hearing brief
CIB	Complainants' initial post-hearing brief
CRB	Complainants' post-hearing reply brief
RPHB	Respondents' pre-hearing brief
RIB	Respondents' initial post-hearing brief
RRB	Respondents' post-hearing reply brief
SPHB	Staff's pre-hearing brief
SIB	Staff's initial post-hearing brief
SRB	Staff's post-hearing reply brief

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation in response to a complaint filed by Complainant Arigna Technology Limited ("Arigna") on May 21, 2021 (the "Complaint," EDIS Doc. ID 743107), and supplemented on May 26, June 9, and June 10, 2021. Notice of Investigation at 1, EDIS Doc. No. 745316 (Jun. 23, 2021); 86 Fed. Reg. 34042 (Jun. 28, 2021). The complaint alleges violations of section 337 of the Tariff Act of 1930, as amended, by reason of infringement of certain claims of U.S. Patent No. 8,247,867 ("the '867 patent") and U.S. Patent No. 8,289,082 ("the '082 patent"). *Id*. The Commission ordered institution of this investigation to determine "whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain products . . . by reason of infringement of one or more of claims 1, 2, 8, and 9 of the '867 patent and claims 1-6, 13, 17-22, and 29 of the '082 patent; and whether an industry in the United States exists as required by subsection (a)(2) of section 337." *Id.* at 2. The investigation was instituted upon publication of the Notice of Investigation in the *Federal Register* on Monday, June 28, 2021. 86 Fed. Reg. 34042-43. The Notice of Investigation named the following entities as Respondents: Volkswagen AG, Volkswagen Group of America, Inc., Audi AG, Audi of America, Bentley Motors Limited, Bentley Motors, Inc., Automobili Lamborghini America, LLC, Automobili Lamborghini S.p.A., Porsche AG, Porsche Cars North America, Inc., Daimler AG, Mercedes-Benz USA, LLC, Bayerische Motoren Werke AG, BMW of North America, LLC, General Motors Company, and General Motors LLC. *Id.* The Office of Unfair Import Investigations is also a party to the investigation. *Id.*

Pursuant to Order No. 5, EDIS Doc. ID. 747201 (Jul. 19, 2021), the target date of this investigation was originally set to be November 28, 2022. *See* Comm'n Notice, EDIS Doc. ID 748429 (Aug. 2, 2021). On September 13, 2021, the investigation was assigned by former Chief Administrative Law Judge Bullock to the undersigned. *See* Notice to the Parties, EDIS Doc. ID 751528 (Sept. 13, 2021).

A *Markman* hearing was held on December 1, 2021. *See Markman* Tr., EDIS Doc. ID 757895 (Dec. 1, 2021). A *Markman* order issued on January 18, 2022, construing certain terms of the asserted claims of the '867 patent and '082 patent. Order No. 30, EDIS Doc. ID 760711.

Pursuant to Order No. 23, EDIS Doc. ID 758896 (Dec. 20, 2021), Arigna withdrew its allegations against Respondent General Motors Company. *See* Comm'n Notice, EDIS Doc. ID 760698 (Jan. 18, 2022). Pursuant to Order No. 37 (Feb. 18, 2022), Arigna withdrew its allegations of infringement with respect to the '867 patent against Respondents BMW AG and BMW of North America, LLC. *See* Comm'n Notice, EDIS Doc. ID 765434 (Mar. 15, 2022). Pursuant to Order No. 50 (Apr. 6, 2022), Arigna withdrew its allegations of infringement with respect to claims 2-6 and 18-22 of the '082 patent and claims 1, 2, and 9 of the '867 patent. *See* Comm'n Notice, EDIS Doc. ID 769133 (Apr. 25, 2022). Pursuant to Order No. 53 (Apr. 29, 2022), Respondents Porsche AG and Porsche Cars North America, Inc. were terminated from the investigation pursuant to a settlement agreement. *See* Comm'n Notice, EDIS Doc. ID 770942 (May 17, 2022).

An evidentiary hearing was held on April 4-8, 2022. The parties filed initial post-hearing briefs on April 25, 2022, and filed post-hearing reply briefs on May 4, 2022. Pursuant to Order No. 54, the target date was extended by two weeks to December 12, 2022. Order No. 54, EDIS Doc. ID 776314 (Jul. 27, 2022).

B. The Parties

1. Complainant

The complainant is Arigna Technology Limited ("Arigna"). Notice of Investigation at 2. Arigna is an Irish company with an address in Dublin, Ireland. Complaint ¶ 7. Arigna is the owner of both the '867 patent and the '082 patent by assignment. *See* JX-00001 ('867 patent assignment abstract); JX-00003 ('867 patent assignment records); JX-00005 ('082 patent assignment records).

2. Third-Party Licensee

Third-party Microchip Technology, Inc. ("Microchip") is a U.S. company headquartered in Chandler, Arizona. *See* CX-00440 (Microchip Form 10-K). Microchip was a previous assignee of the '082 patent. *See* JX-00005. Arigna has granted Microchip a license to the '082 patent and the '867 patent. CX-00097C (Arigna-Microchip Agreement, June 26, 2020).

3. Respondents

The respondents are vehicle manufacturers. *See* RIB at 4.

Respondent Bayerische Motoren Werke AG ("BMW AG") is a German company with its principal place of business in Munich, Germany. BMW AG Answer to Complaint at ¶ 15, EDIS Doc. ID 748293 (Jul. 29, 2021). BMW of North America, LLC ("BMW NA") is an indirect subsidiary of BMW AG (together, BMW AG and BMW NA are "BMW"), with a principal place of business in Woodcliff Lake, New Jersey. BMW NA Answer to Complaint at ¶ 15, EDIS Doc. ID 748281 (Jul. 29, 2021).

Respondent General Motors LLC ("GM" or "General Motors") is a Delaware corporation headquartered in Detroit, Michigan. GM Answer to Complaint at ¶ 21, EDIS Doc. ID 748267 (Jul. 29, 2021).

Respondent Daimler AG ("Daimler") is a German corporation headquartered in Stuttgart, Germany. Daimler Answer to Complaint at ¶ 27, EDIS Doc. ID 748569 (Jul. 29, 2021). Respondent Mercedes-Benz USA, LLC ("MBUSA") is a Delaware company headquartered in Sandy Springs, Georgia. MBUSA Answer to Complaint at ¶ 27, EDIS Doc. ID 748564 (Jul. 29, 2021). MBUSA is owned by Daimler International Nederland B.V., which is a wholly-owned subsidiary of Daimler (together, Daimler and MBUSA are "Mercedes"). *See* CX-02300C.

Respondent Volkswagen AG is a German corporation headquartered in Wolfsburg, Germany. Volkswagen Answer to Complaint at ¶ 12, EDIS Doc. ID 748269 (Jul. 29, 2021). Respondent Audi AG is a German corporation located in Ingolstadt, Germany. *Id*. Respondent Audi of America, LLC is a Delaware corporation located in Herndon, Virginia. *Id*. Respondent Bentley Motors Limited is a British corporation located in Cheshire, England. *Id*. at ¶ 18. Respondent Bentley Motors, Inc. is a New York corporation located in Herndon, Virginia. Respondent Volkswagen Group of America, Inc. is a New Jersey corporation located in Herndon, Virginia. *Id*. Respondent Automobili Lamborghini S.p.A., is an Italian corporation located in Bolognese, Italy. *Id*. at ¶ 24. Automobili Lamborghini S.p.A is a wholly owned subsidiary of [redacted] *Id*. Automobili Lamborghini America, LLC is a Delaware corporation located in Herndon, Virginia. *Id*. Automobili Lamborghini America, LLC is a wholly owned subsidiary of [redacted]. *Id*. Respondents Volkswagen AG, Volkswagen Group of America, Inc., Audi AG, Audi of America, LLC, Bentley Motors Limited, Bentley Motors, Inc., Automobili Lamborghini S.p.A., and Automobili Lamborghini America, LLC are collectively the "Volkswagen Group."

C. Products at Issue

The products at issue are "power inverters and converters used in automobiles, components thereof, and automobiles containing those power inverters or converters." Notice of Investigation at 2. Arigna accuses different sets of products of infringing claims of the '082 patent and '867 patent. CIB at 7-9. Arigna also relies on different sets of products for the domestic industry requirement. *Id*. at 9.

1. Accused Products – '082 Patent

Arigna accuses the Hella 48V Converter (containing the Analog Devices AD8417 chip), the Bosch 48V Converter and Bosch LEB450 Inverter (containing the Analog Devices AD8418 chip) of infringing claims 1, 13, 17, and 29 of the '082 patent. CIB at 7-8; Tr. (Sechen) at 165:12-18. The Hella 48V Converter is alleged to be used in certain Mercedes vehicles. CIB at 7-8. The Bosch 48V Converter is alleged to be used in certain Volkswagen vehicles. *Id*. The Bosch LEB450 Inverter is alleged to be used in certain BMW vehicles. *Id*.

2. Accused Products – '867 Patent

Arigna accuses the [redacted], and certain Respondents' electric vehicles containing these inverters, and components thereof, of infringing claim 8 of the '867 patent. CIB at 8-9; Tr. (Sechen) at 312:15-313:5 and CDX-001C.141. Each of the accused inverters and vehicles includes an Infineon IGBT chip. *Id*.[1] The accused [redacted] contains an Infineon TRENCHSTOP 5 chip with part number [redacted]. *Id*. The accused [redacted]

[1] The term "IGBT" means "Insulated Gate Bipolar Transistor." Tr. (Sechen) at 314:7-9; Tr. (Resp. Opening) at 65. The accused chips are IGBTs. *See* Tr. (Sechen) at 448:12-14; RX-0713C ([redacted] Decl.) ¶¶ 3, 20.

Inverter, [redacted] contain [redacted] The accused [redacted] is used in the accused GM Cadillac Lyriq (2022+ models), and the accused [redacted] is used in the accused GM Hummer EV (models 2021+) and BrightDrop EV600 (models 2021+). *Id.* The accused [redacted] are used in the accused VW ID.4 (models [redacted]), Audi [redacted] (models [redacted]), and Audi [redacted] (models [redacted]). *Id.*

3. Domestic Industry Products

The domestic industry products for the '082 patent are Microchip's ATMXT540S and ATMXT336S MaXTouch controllers. CIB at 9. The domestic industry products for the '867 patent are certain Microchip Trench FET products in development, which are identified by their mask numbers: [redacted] *Id.*

D. Asserted Patents

The '082 patent is titled "Circuit and Method for Adjusting an Offset Output Current for an Input Current Amplifier" and was originally assigned to Atmel Corporation, a predecessor-in-interest to Microchip. *See* JX-00005 ('082 assignment records).

[2] "EDT2" and "TRENCHSTOP 5" are two categories of Infineon IGBT chips. RX-0713C ([redacted] Decl.) ¶¶ 3, 20.

The ’867 patent is titled “Semiconductor Device” and was originally assigned to Mitsubishi Electric Corporation (“Mitsubishi”). JX-00004. Arigna acquired ownership of the ’867 patent from Mitsubishi on February 13, 2020. JX-00001.

E. Witness Testimony

The undersigned received testimonial evidence in this investigation in the form of live testimony and deposition designations.

1. Hearing Testimony

Arigna relies on the testimony of Dr. Carl Sechen, who was admitted as an expert in the field of electrical engineering, including analog circuit and semiconductor design and fabrication. Tr. at 154:20-155:13. Dr. Sechen offered testimony regarding the alleged infringement and satisfaction of the technical prong of the domestic industry requirement with respect to the asserted claims of the ’082 patent and ’867 patent,. *Id*. at 148-611. He also offered testimony regarding the validity of the asserted claims of the ’082 patent and ’867 patent. *Id*. at 1221-1310. Arigna also relies on the testimony of Mr. Gregory Smith, who was admitted as an expert in the field of economics to offer economic analysis on issues related to domestic industry, public interest, and remedy. Tr. at 612-712 (expert qualification at 616:10-25).

Respondents rely on the testimony of Dr. John Bravman, who was admitted as an expert in the field of semiconductor device structures, semiconductor device fabrication, semiconductor device imaging, and characterization and related technology and offered testimony regarding the ’867 patent. Tr. at 714-940 (expert qualification at 719:8-20). Respondents also rely on the testimony of Mr. Brett Reed, who was admitted as an expert in economics, particularly with issues relevant to section 337 investigations. Tr. at 942-989 (expert qualification at 944:22-945:10). Respondents further rely on the testimony of Dr. John Graham, who was admitted as an

expert in the area of public policy, public health, cost-benefit analysis, regulatory and policy analysis relating to electrified vehicles. Tr. at 990-1025 (expert qualification at 993:1-15). Respondents also rely on the testimony of Dr. Nareg Sinenian, who was admitted as an expert in the field of design and analysis of electronic circuits, including amplifiers and offered testimony regarding the alleged infringement of the asserted claims of the '082 patent. Tr. at 1026-1111 (expert qualification at 1032:9-21). Respondents' final witness was Dr. Shoukri Souri, who was admitted as an expert in the field of design and analysis of electronic circuits, including amplifiers and offered testimony regarding the asserted invalidity of the '082 patent. Tr. at 1112-1221 (expert qualification at 1116:22-1117:6).

2. Deposition Designations and Declarations

The parties submitted several designated deposition transcripts and third-party declarations, which were received in evidence without a sponsoring witness. Tr. at 527:1-17.

Exhibit	Description
JX-00010C	2021-12-08 Designated Deposition Transcript of [redacted]
JX-00011C	2021-12-02 Designated Deposition Transcript of [redacted]
JX-00012C	2021-12-08 Designated Deposition Transcript of Thomas Danieli
JX-00013C	2021-12-10 Designated Deposition Transcript of [redacted]
JX-00014C	2021-12-14 Designated Deposition Transcript of Stephanus Duvenhage
JX-00015C	2021-12-03 Designated Deposition Transcript of [redacted]
JX-00016C	2021-12-10 Designated Deposition Transcript of Rudy Jaramillo
JX-00017C	2021-12-08 Designated Deposition Transcript of Paul Kelley
JX-00018C	2021-12-14 Designated Deposition Transcript of Leonardo Laviola
JX-00019C	2021-12-09 Designated Deposition Transcript of [redacted]
JX-00020C	2021-12-07 Designated Deposition Transcript of [redacted]
JX-00021C	2021-12-10 Designated Deposition Transcript of [redacted]
JX-00022C	2021-11-23 Designated Deposition Transcript of [redacted]
JX-00023C	2021-12-09 Designated Deposition Transcript of Michael Rocco
JX-00024C	2022-01-19 Designated Deposition Transcript of [redacted]
JX-00025C	2021-12-14 Designated Deposition Transcript of Patrick Stowe
JX-00026C	2021-12-20 Designated Deposition Transcript of Gerald Padian
CX-00519C	Declaration of Steve Liu on behalf of Delta Electronics
CX-00520C	Declaration of Alasdair Alexander on behalf of Analog Devices, Inc.
CX-00521C	Declaration of [redacted]on behalf of Hella GmbH

CX-00522C	Declaration of Carlos Sanchez on behalf of Analog Devices, Inc.
CX-00523C	Declaration of Seungyu Yoon on behalf of LG Magna

II. JURISDICTION

In order to have the power to decide a case, a court or agency must have both subject matter jurisdiction and jurisdiction over either the parties or the property involved. 19 U.S.C. § 1337; *Certain Steel Rod Treating Apparatus and Components Thereof*, Inv. No. 337-TA-97, Commission Memorandum Opinion, 215 U.S.P.Q. 229, 231 (1981).

A. Subject Matter Jurisdiction

Section 337 confers subject matter jurisdiction on the Commission to investigate, and if appropriate, to provide a remedy for, unfair acts and unfair methods of competition in the importation, the sale for importation, or the sale after importation of articles into the United States. *See* 19 U.S.C. §§ 1337(a)(1)(B) and (a)(2). The Commission has subject matter jurisdiction over this investigation based on Arigna's allegations that the accused products are imported into the United States. CIB at 10; RIB at 15; *see Amgen Inc. v. Int'l Trade Comm'n*, 565 F.3d 846, 854 (Fed. Cir. 2009) ("In this case, the Commission had jurisdiction as a result of Amgen's allegation that Roche imported an article . . . covered by the claims of a valid and enforceable United States patent.").

B. Personal Jurisdiction

Respondents have submitted to the personal jurisdiction of the Commission by answering the Complaint and Notice of Investigation, participating in discovery, appearing at hearings, and filing motions and briefs. *See Certain Miniature Hacksaws*, Inv. No. 337-TA-237, USITC Pub. No. 1948, Initial Determination at 4, 1986 WL 379287, *1 (Oct. 15, 1986), *not reviewed in relevant part by* Comm'n Action and Order, 1987 WL 450871 (Jan. 15, 1987). Respondents do not contest that the Commission has *in personam* jurisdiction over them. RIB at 15.

C. *In Rem* Jurisdiction

The Commission has *in rem* jurisdiction over accused products by virtue of their importation into the United States. *See Sealed Air Corp. v. U.S. Int'l Trade Comm'n*, 645 F.2d 976, 985-86 (C.C.P.A. 1981) (holding that the ITC's jurisdiction over imported articles is sufficient to exclude such articles). Except for a dispute regarding certain types of accused chips used in the accused VW vehicles, Respondents have admitted to the importation of the accused vehicles and/or components. *See* CX-00515C (GM Joint Stipulation of Facts); CX-00027C (Audi Interrogatory Response); CX-01948C (BMW Joint Stipulation); CX-02253C (Bentley Interrogatory Response); CX-00120C (Lamborghini Interrogatory Response); CX-02300C (Mercedes Interrogatory Response); CX-02370C (VW Interrogatory Response).[3]

III. LEGAL STANDARDS

A. Infringement

Section 337(a)(1)(B)(i) prohibits "the importation into the United States, the sale for importation, or the sale within the United States after importation by the owner, importer, or consignee, of articles that – (i) infringe a valid and enforceable United States patent or a valid and enforceable United States copyright registered under title 17." 19 U.S.C. §1337(a)(1)(B)(i). The Commission has held that the word "infringe" in Section 337(a)(1)(B)(i) "derives its legal meaning from 35 U.S.C. § 271, the section of the Patent Act that defines patent infringement." *Certain Elec. Devices with Image Processing Sys., Components Thereof, and Associated Software*, Inv. No. 337-TA-724, Comm'n Op. at 13-14, EDIS Doc. ID 467105 (December 21, 2011).

[3] VW disputes whether certain types of accused chips have been imported, as discussed in Part V.E *infra*.

Infringement must be proven by a preponderance of the evidence. *SmithKline Diagnostics, Inc. v. Helena Labs. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). The preponderance of the evidence standard "requires proving that infringement was more likely than not to have occurred." *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n.15 (Fed. Cir. 2005). Literal infringement requires the patentee to prove that the accused device meets each and every limitation of the asserted claim(s). *Frank's Casing Crew & Rental Tools, Inc. v. Weatherford Int'l, Inc.*, 389 F.3d 1370, 1378 (Fed. Cir. 2004). "If even one limitation is missing or not met as claimed, there is no literal infringement." *Elkay Mfg. Co. v. EBCO Mfg. Co*., 192 F.3d 973, 980 (Fed. Cir. 1999). Literal infringement is a question of fact. *Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008).

B. Claim Construction

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996) (citation omitted). "[T]he construction of claims is simply a way of elaborating the normally terse claim language[] in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000) (alterations in original) (quoting *Scripps Clinic v. Genentech, Inc.*, 927 F.2d 1565, 1580 (Fed. Cir. 1991)). "[O]nly those [claim] terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy." *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). The words of a claim "'are generally given their ordinary and customary meaning,'" which is "the meaning that the term would have to a person of ordinary skill in art"

as of the date that the patent application was filed. *Phillips v. AWH Corp.,* 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

C. Invalidity

It is the respondents' burden to prove invalidity, and the burden of proof never shifts to the patentee to prove validity. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1380 (Fed. Cir. 2008). "Under the patent statutes, a patent enjoys a presumption of validity, *see* 35 U.S.C. § 282, which can be overcome only through facts supported by clear and convincing evidence . . . ." *SRAM Corp. v. AD-II Eng'g, Inc.*, 465 F.3d 1351, 1357 (Fed. Cir. 2006); *see also Microsoft Corp. v. i4i Ltd. P'ship*, 564 U.S. 91, 100-114 (2011) (upholding the "clear and convincing" standard for invalidity).

The clear and convincing evidence standard placed on the party asserting an invalidity defense requires a level of proof beyond the preponderance of the evidence. Although not susceptible to precise definition, "clear and convincing" evidence has been described as evidence that produces in the mind of the trier of fact "an abiding conviction that the truth of a factual contention is 'highly probable.'" *Price v. Symsek*, 988 F.2d 1187, 1191 (Fed. Cir. 1993) (quoting *Buildex, Inc. v. Kason Indus., Inc.,* 849 F.2d 1461, 1463 (Fed. Cir. 1988)).

1. Anticipation

Pursuant to 35 U.S.C. § 102, a patent claim is invalid as anticipated if:

> (1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention; or
>
> (2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be,

> names another inventor and was effectively filed before the effective filing date of the claimed invention.

35 U.S.C. § 102 (2012). "A patent is invalid for anticipation if a single prior art reference discloses each and every limitation of the claimed invention. Moreover, a prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference." *Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003) (citations omitted).

2. Obviousness

Section 103 of the Patent Act states:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

35 U.S.C. § 103(a) (2011).

"Obviousness is a question of law based on underlying questions of fact." *Scanner Techs.*, 528 F.3d at 1379. The underlying factual determinations include: "(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness." *Id.* at 1380 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)). These factual determinations are often referred to as the "*Graham* factors."

A relevant inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-21 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit's

rigid application of the teaching-suggestion-motivation test. While the Court stated that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does," it described a more flexible analysis:

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue . . . . As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 418. Applying *KSR*, the Federal Circuit has held that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device . . . and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

In addition to demonstrating that a reason exists to combine prior art references, the challenger must demonstrate that the combination of prior art references discloses all of the limitations of the claims. *Hearing Components, Inc. v. Shure Inc.*, 600 F.3d 1357, 1373-1374 (Fed. Cir. 2010), *abrogated on other grounds by Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014) (upholding finding of non-obviousness based on substantial evidence that the asserted combination of references failed to disclose a claim limitation); *Velander v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (explaining that a requirement for a finding of obviousness is that "all the elements of an invention are found in a combination of prior art references").

3. Indefiniteness

"The Patent Act requires that a patent specification 'conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as [the] invention.'" *Nautilus, Inc. v. Biosig Instruments, Inc.,* 572 U.S. 898 (2014) (quoting 35 U.S.C. § 112, ¶ 2). "[T]he second paragraph of § 112 contains two requirements: first, [the claim] must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g Corp. v. Bartell Indus., Inc,.* 299 F.3d 1336, 1348 (Fed. Cir. 2002) (citation and internal quotation marks omitted) (alteration in original). A claim does not satisfy the second requirement and is thereby indefinite "if read in light of the specification delineating the patent, and the prosecution history, [the claim] fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus*, 534 U.S. at 901. Indefiniteness is a question of law, subject to a determination of underlying facts. *Akzo Nobel Coatings, Inc. v. Dow Chem. Co.,* 811 F.3d 1334, 1343-44 (Fed. Cir. 2016). The party challenging the validity of a claim bears the burden of establishing indefiniteness. *Id*.

D. Domestic Industry

In patent-based proceedings under section 337, a complainant must establish that an industry "relating to the articles protected by the patent . . . exists or is in the process of being established" in the United States. 19 U.S.C. § 1337(a)(2). Under Commission precedent, the domestic industry requirement of section 337 consists of a "technical prong" and an "economic prong." *See, e.g., Alloc, Inc. v. Intl Trade Comm'n,* 342 F.3d 1361, 1375 (Fed. Cir. 2003).

To meet the technical prong, the complainant must establish that it practices at least one claim of the asserted patent. *Certain Point of Sale Terminals and Components Thereof*, Inv. No.

337-TA-524, Order No. 40 at 17-18, EDIS Doc. ID 230409 (Apr. 11, 2005). "The test for satisfying the 'technical prong' of the industry requirement is essentially [the] same as that for infringement, *i.e.*, a comparison of domestic products to the asserted claims." *Alloc*, 342 F.3d at 1375.

With respect to the "economic prong," subsection (3) of Section 337(a) provides:

> For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned –
>
> (A) significant investment in plant and equipment;
>
> (B) significant employment of labor or capital; or
>
> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3).

Under subsections (A) and (B), the economic prong focuses on "articles protected by the patent." *Id*. Expenditures may be counted toward satisfaction of the domestic industry requirement "as long as those investments pertain to the complainant's industry with respect to the articles protected by the asserted IP rights." *Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Comm'n Op. at 68, 2015 WL 6755093, at *36 (Oct. 30, 2015); *accord, e.g., Certain Marine Sonar Imaging Devices, Including Downscan and Sidescan Devices, Prods. Containing the Same, and Components Thereof*, Inv. No. 337-TA-921, Comm'n Op., 2016 WL 10987364, at *40 (Jan. 6, 2016) ("Navico's allocation methodology reasonably approximates the warranty and technical customer support expenditures relating to the LSS-1 product.") (*citing Certain Ground Fault Circuit Interrupters and Prods. Containing Same,* Inv. No. 337-TA-739, Comm'n Op. at 74-75, 79-81, EDIS Doc. ID 482482 (June 8, 2012)).

Whether a complainant satisfies the economic prong is not analyzed according to a rigid mathematical formula. *Certain Male Prophylactic Devices*, Inv. No. 337-TA-546, Comm'n Op. at 39, EDIS Doc. ID 279161 (Aug. 1, 2007). The decision is made on a case-by-case basis and requires "an examination of the facts in each investigation, the article of commerce, and the realities of the marketplace." *Id.* A complainant must "provide context of the company's operations, the marketplace, or the industry in question necessary to understand whether the value of its domestic activities is significant or substantial." *Certain Carburetors and Products Containing Such Carburetors*, Inv. No. 337-TA-1123, Comm'n Op. at 19, EDIS Doc. ID 692517 (Oct. 28, 2019). However, there is no "minimum monetary expenditure," and a complainant does not "need to define or quantify the industry itself in absolute mathematical terms." *Stringed Musical Instruments,* Inv. No. 337-TA-586, Comm'n Op., 2009 WL 5134139, at *16 (December 2009). "A precise accounting [of the complainant's domestic investments] is not necessary, as most people do not document their daily affairs in contemplation of possible litigation." *Id*. at 17.

IV. U.S. PATENT NO. 8,289,082

The '082 patent (JX-00006) is titled "Circuit and Method for Adjusting an Offset Output Current for an Input Current Amplifier" and names Armin Prohaska, Terje Saether, and Holger Vogelmann as inventors. '082 patent, cover. The '082 patent issued from an application filed on December 22, 2010, and claims priority to a provisional application filed on December 23, 2009. *Id*.

A. Specification

The ’082 patent describes an invention for correcting an undesirable offset at the output of a current amplifier. ’082 patent, Abstract. An exemplary embodiment shows a circuit diagram for an input current amplifier 100 with an adjusting circuit 200. *Id*. at 5:50-55.

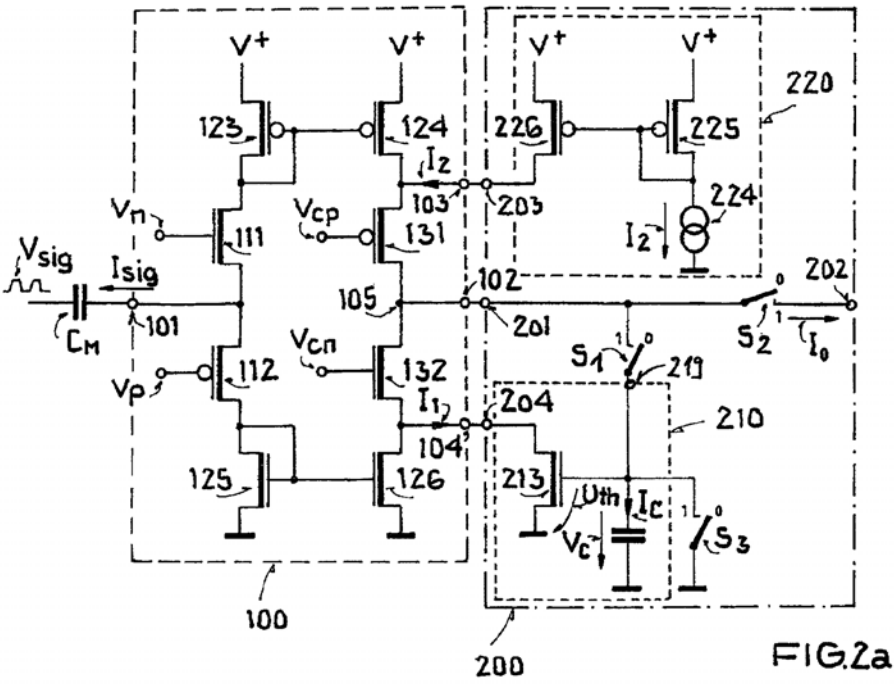

FIG.2a

Id. at Fig. 2a. “Because of process deviations during production,” the output of the current amplifier 100 has an offset “Ioff.” *Id*. at63-67. “Preferably, the adjusting circuit 200 is formed to adjust the offset Ioff of the current amplifier 100 to a minimum, preferably to the value of zero.” *Id*. at 6:17-19. The adjusting circuit 200 is comprised of two current sources, a controlled current source 210 and a constant current source 220, which are both connected to the output of the current amplifier 100. *Id*. at 6:19-54.

The adjusting circuit further includes switching devices that can be opened and closed by signals from a control circuit for different states of operation. *Id*. at 7:36-67, 9:44-64. “In the closed state, first switching device S1 connects output 102 of adjusting circuit 200 to input 219

of controlled current source 210 and forms a control loop, whereby controlled current source 210 acts as a regulation element of this control loop." *Id*. at 7:45-49. "For regulation, second switching device S2 is open and disconnects output 202 of the circuit from output 102 of the adjusting circuit 200." *Id*. at 7:58-67. The capacitor 212 is charged by charging current Ic, which sets a current value of output current I1 such that "the offset Ioff active at output 102 is regulated to a minimum and thereby to a constant value, ideally zero." *Id*. at 8:1-13.

B. Asserted claims

Arigna asserts claims 1, 13, 17, and 29 of the '082 patent. *See* Order No. 50 at 3 n.4. These claims are recited below:

> 1. A circuit comprising:
>
> a current amplifier; and
>
> an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device,
>
> wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier,
>
> wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop,
>
> wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element,
>
> wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current, and
>
> wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current.
>
> 13. The circuit according to claim 1, further comprising a control circuit that is configured to control the first switching device and is connectable to a control terminal of the first switching device.

17. A method for correcting an offset of an output current of a current amplifier of a circuit, the method comprising:

connecting a controlled current source to an output of the current amplifier via a first switching device, to form a regulation element of a control loop;

regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element; and

disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current.

29. The method according to claim 17, further comprising a control circuit that is configured to control the first switching device and is connectable to a control terminal of the first switching device.

C. Claim Construction

The parties agreed to the construction of several claim terms in the '082 patent. *See* Updated Joint Proposed Claim Construction Chart, EDIS Doc. ID 758271 (Dec. 9, 2021). The parties agreed that the term "current amplifier" has its "plain and ordinary meaning, *e.g.*, an amplifier that takes an input current and outputs an amplified current." *Id*. at 3. The parties agreed that the term "output of the current amplifier" has its plain and ordinary meaning, and the term "output current of a current amplifier" also has its "plain and ordinary meaning, *e.g.*, the amplified current output by the amplifier." *Id*. The term "the output current," as used in the asserted claims, was agreed to have its plain and ordinary meaning, *i.e.*, "the output current of the controlled current source." The term "offset of an output current of [the/a] current amplifier" was agreed to mean the "difference between observed and desired output current of [the/a] current amplifier." *Id*. at 4.

In the *Markman* order, the preamble of claim 17 was found to be limiting. Order No. 30 at 31-36. The parties were asked to provide additional briefing on the construction of the term

"input signal of the current amplifier." *Id.* at 36-39; *see* CIB at 12-18; RIB at 17-19; SIB at 33-37. The parties also dispute the construction of the terms "regulate the offset to a minimum" in claim 1 and "regulating the offset to a minimum" in claim 17. *See* Updated Joint Proposed Claim Construction Chart at 4; CIB at 18-22; RIB at 15-17; SIB at 40-43.

1. "input signal of the current amplifier"

The parties dispute the construction of the term "input signal of the current amplifier" in claim 17 of the '082 patent.

Complainant's Construction	Respondents' Construction	Staff's Construction
Plain and Ordinary Meaning	"current supplied to the current amplifier for current amplification"	Plain and ordinary meaning

The key dispute among the parties regarding this term is whether the "input signal of the current amplifier" can be a voltage signal, or whether it must be a current signal. Arigna submits that this term should have its plain and ordinary meaning, which it argues can refer to a voltage input to the claimed current amplifier. CIB at 12-18; CRB at 20-24. Respondents argue that the term refers to a current, and propose to construe "input signal of the current amplifier" to refer to the "current supplied to the current amplifier for current amplification." RIB at 17-19; RRB at 3-7. Staff agrees with Arigna that the "input signal of the current amplifier" is not necessarily a current. SIB at 33-37.

Claim 17 describes "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value." Respondents argue that this "regulation phase" corresponds to a description in the specification where the input current signal has a constant value, preferably zero, and this is summed with the output current and constant current to determine the appropriate level of offset

correction. '082 patent at 7:58-67; *see* RIB at 17-18. "The regulation occurs when an input signal of the current amplifier has a constant value . . . Ideally, the direct current value, present at the input of the current amplifier, of the input signal is zero." '082 patent at 2:23-30 (cited in RIB at 18). Respondents' expert Dr. Sinenian submits that "what a person of ordinary skill would understand in reading this part of the specification is that during this regulation phase, the input signal is a current." Tr. (Sinenian) at 1066:9-1068:17.

Dr. Sinenian further submits that a "current amplifier" is one type of fundamental amplifier, referencing electrical engineering textbooks (including the figure reproduced below). *Id*. at 1033:4-1038:14.; RDX-0005C.4. He explains that "a current amplifier has a current signal as its input." *Id*. at 1036:25-1037:16.

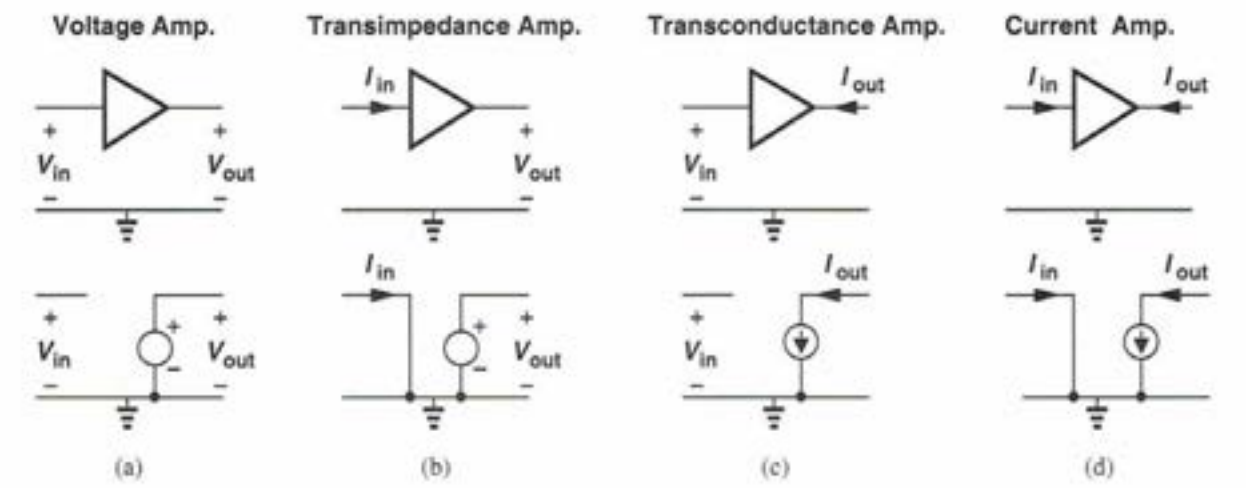

Figure 8.11 Types of amplifiers along with their idealized models.

RX-1629 (Razavi, "Design of Analog CMOS Integrated Circuits") at 254; *see also* RX-1630 (Sedra and Smith, "Microelectronic Circuits") at 28. The '082 patent specification states: "Current amplifier 100 has a current input and a current output." '082 patent at 5:34-35; *see* RIB at 17. Arigna's expert Dr. Sechen agrees that a current amplifier "is an amplifier that receives an input current and outputs a current that is larger than the input current." Tr. (Sechen) at 158:24-

159:3. Staff agrees that this understanding of a "current amplifier" is consistent with the specification and the extrinsic evidence. SIB at 29-32.

Although the parties agree that a "current amplifier" receives an input current, Arigna argues that the claim language "input signal of the current amplifier" is broad enough to encompass other inputs, including voltage signals. CIB at 12-18; CRB at 20-24. Dr. Sechen submits that this is consistent with the specification of the '082 patent, which identifies a voltage signal "Vsig" as an input signal that is used to create the "Isig" current that is input to the current amplifier 100. Tr. (Sechen) at 160:24-161:19. He submits that when "Vsig" is constant, the corresponding "Isig" will be zero. *Id*. at 249:8-16. Dr. Sechen suggests that the voltage signal "Vsig" is constant during the "regulation period" depicted in Figure 2b of the '082 patent, a timing diagram that describes the operation of several switches. *Id*. at 248:8-250:2.

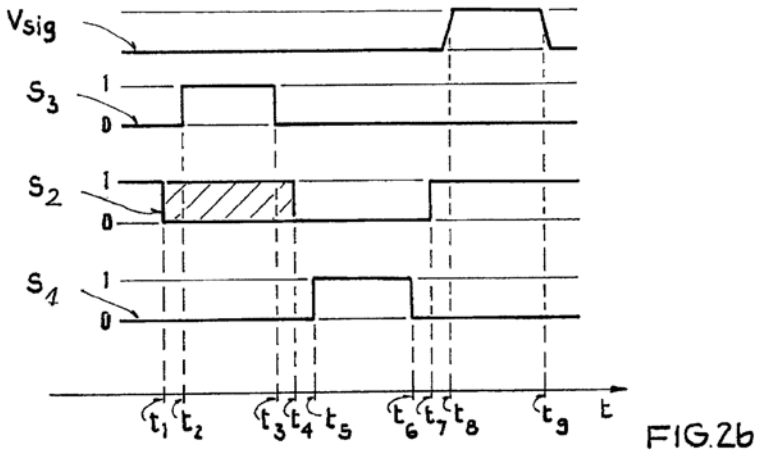

FIG.2b

'082 patent, Fig. 2b. Arigna identifies a statement in the specification that states: "For regulation, second switching device S2 is open." *Id*. at 7:58-60. Arigna submits that in Figure 2b, Vsig is constant between t1 and t7, when S2 is open. CIB at 16. Arigna argues that Respondents' proposed construction would exclude the embodiment depicted in Figure 2b by

limiting the "input signal" to the current signal Isig, because Isig is zero and a zero signal cannot be amplified. *Id*. at 17-18.

Respondents argue that Vsig cannot be the claimed "input signal" because it is not input to the current amplifier 100. RIB at 18-19. Dr. Sinenian explains that the role of Vsig is only to power the capacitor Cm, which generates the signal Isig when the user interacts with the touchscreen. Tr. (Sinenian) at 1068:25-1069:17. He also testifies that in the device depicted in the specification, Vsig does not "enter the amplifier" and "does not carry information that is amplified by the current amplifier." *Id*. at 1069:18-21. As described in the specification in reference to Figure 2b, "[b]etween time points t8 and t9, a voltage signal Vsig is sent to a capacitor Cm of a touch screen. If the screen is touched, the capacitor Cm is changed and moreover a signal current Isig is produced, which flows as an input current via input 101 into/out of input current amplifier 100 and is amplified by input current amplifier 100." '082 patent at 8:57-62. Respondents submit that a zero Isig signal as input to the current amplifier during the regulation phase is consistent with the explicit disclosure of the specification. RRB at 5-6; '082 patent at 7:58-61 ("For regulation . . . [t]he input signal current Isig is zero in this case.").

Staff agrees with Respondents that the "input signal" of the current amplifier described in the preferred embodiments of the specification is "the current that is input into the amplifier for current amplification" (SIB at 33), but Staff argues that the scope of the claim should not be limited to the preferred embodiment. SIB at 33-37. Staff identifies disclosures in the specification that use the terms "input" and "signal" to refer to other types of electrical inputs and signals. *Id*. at 34. In particular, the specification describes "voltage signal Vsig" that is "sent to a capacitor Cm of a touch screen." '082 patent at 8:57-58. In addition, there is a "control signal" sent by control circuit 300 to switching device S2 and S3. *Id*. at 9:34-41. The

specification also refers to "a control voltage at the control input of the transistor" in the controlled current source. *Id*. at 2:60-62. Staff argues that claim 17 uses the terms "output current" and "current value" but does not refer to the "input signal" as an "input current," suggesting that the "input signal" could be something other than a current. SIB at 34-35. Staff argues that Respondents' construction would improperly limit the claimed current amplifier to only one input. *Id*. at 36-37.

In consideration of the parties' arguments, the undersigned finds that the term "input signal of the current amplifier," viewed in light of the claim language, specification and the plain and ordinary meaning of "current amplifier," refers to a current signal. With regard to the current amplifier, the specification of the '082 patent only uses the term "input signal" to refer to a current, which is identified as "Isig." *See* '082 patent at 1:64-67, 2:10-13, 2:26-32, 2:37-40, 7:2-5, 7:58-61. In the context of regulating an offset to a minimum, the specification explains why this "input signal" must be constant or zero:

> The regulation occurs when an input signal of the current amplifier has a constant value. Therefore, only a direct current value but not an alternating current is present at the input of the current amplifier during the regulation. Ideally, the direct current value, present at the input of the current amplifier, of the input signal is zero.

Id. at 2:26-32.[4] In the alleged invention disclosed in the '082 patent, the amount of offset to be corrected is determined when the input signal of the current amplifier is constant or zero, because this permits one to expose the undesired offset current and correct for it. *See* Tr. (Sinenian) at 1066:9-1067:15. There is no embodiment of the invention disclosed in the '082 patent where

[4] *See also id*. at 7:58-65 ("For regulation, second switching device S2 is open and disconnects output 202 of the circuit from output 102 of adjusting circuit 200. The input signal current Isig is zero in this case. As a result, the resulting current, which results from the summation of the output current of first current mirror 123, 124, of the output current of second current mirror 125, 126, and of constant current I2, flows out at output 102 of input current amplifier 100.").

regulating an offset of the current amplifier is associated with keeping a different input signal of the current amplifier constant, such as the control signals identified by Staff. *See* SIB at 33 ("in the preferred embodiments, the 'input signal' is identified as the current that is input into the amplifier for current amplification."). The claim describes "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value," and the only "input signal" that makes sense in the context of the specification, the claim language, and the accepted meaning of "current amplifier," is a current signal. *See* Tr. (Sinenian) at 1033:4-1038:14; RX-1629 (Razavi, "Design of Analog CMOS Integrated Circuits") at 254; RX-1630 (Sedra and Smith, "Microelectronic Circuits") at 28; '082 patent at 5:34-35; Tr. (Sechen) at 158:24-159:3 (current amplifier "is an amplifier that receives ***an input current*** and outputs a current that is larger than the input current") (emphasis added).

Arigna's arguments regarding "Vsig" are unpersuasive because "Vsig" is not input to the current amplifier in the specification. *See* '082 patent at Fig. 2a; *see also* Tr. at 1069:22-1070:1 (Q: "Does Vsig even enter the current amplifier?" A (Sinenian): "No. Again, Cm represents the touchscreen controller in this case. I believe the specification calls that out. So it is not even connected to the input directly. It is connected to the touchscreen controller."); SIB at 33.

While the undersigned agrees with Staff that the terms "input" and "signal," in isolation, can have broader meanings in the art, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention" requires an input signal that is a current. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). In addition, the undersigned is persuaded by Dr. Sinenian's testimony that one of ordinary skill in the art would read the term "input signal of the current amplifier" in the context

of the '082 patent to refer to a current signal. *See* Tr. (Sinenian) at 1066:9-1068:17. This construction, moreover, does not mean that the term "input signal" lacks any meaning beyond being an "input current." Rather the word "signal" indicates that it is an input current carrying information of interest. *See* SMX-0006, Penguin Dictionary of Electronics, 3rd ed. (1998) (EDIS Doc. ID 756132) at 515 ("signal" is a variable electrical parameter "used to convey information"); Tr. (Sinenian) at 1033:10 ("a signal carries information of interest"); Tr. (Souri) at 1168:6-13 (stating that signals carry or can carry "meaningful information" and distinguishing between "input signal of the current amplifier" and noise); SIB at 52 (stating that a "signal" is used to convey "some information of interest" and distinguishing between a "current signal" and a current value derived for a voltage signal through Ohm's law).

For these reasons, the term "input signal of the current amplifier," as used in claim 17 of the '082 patent, refers to a current, not a voltage.[5]

2. "regulat[ing] the offset to a minimum"

The parties dispute the construction of the terms "regulate the offset to a minimum" in claim 1 and "regulating the offset to a minimum" in claim 17 of the '082 patent.

Complainant's Construction	Respondents' Construction	Staff's Construction
"adjust the offset to a value closer to zero" / "adjusting an offset to a value closer to zero"	Indefinite	"regulating an offset to at or near zero"

[5] For purposes of assessing the disputed infringement and invalidity issues, it is unnecessary to resolve other disputes among the parties regarding the proper construction—*e.g.*, whether the current that is the "input signal of the current amplifier" must undergo current amplification during the regulation phase. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd. Matal.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("we need only construe terms that are in controversy, and only to the extent necessary to resolve the controversy") (internal citations omitted); *see also Choon's Design, LLC v. Idea Village Prods. Corp.*, 776 Fed. Appx. 691 n.3 (Fed. Cir. June 24, 2019).

Respondents contend that the terms "regulate the offset to a minimum" and "regulating the offset to a minimum" are indefinite. RIB at 15-17; RRB at 7-8. Arigna proposes to construe these terms to mean "adjust the offset to a value closer to zero" or "adjusting an offset to a value closer to zero." CIB at 18-22; CRB at 24-28. Staff proposes its own construction of these terms: "regulating an offset to at or near zero." SIB at 40-43; SRB at 10-11.

Respondents argue that these terms are indefinite because there are no objective boundaries for the claimed "minimum." RIB at 15-17; RRB at 7-8. Respondents' expert Dr. Souri offered his opinion that these terms are indefinite because there is no indication in the specification that provides reasonable certainty for the range of values that would be a "minimum" and submits that this is not a term of art. Tr. (Souri) at 1184:10-1185:14.

Arigna argues that these terms are not indefinite because the specification explicitly provides that "[t]he minimum offset is achieved when the output current from a current amplifier has reached a steady state; therefore it is substantially constant, ideally zero." '082 patent at 2:3-6. Dr. Sechen testified at the hearing that the term "steady state" means "when current and voltage values are no longer varying. They're constant, in other words." Tr. (Sechen) at 206:14-20. Dr. Sechen further explained that "at the schematic level, if you were to simulate the circuit with a standard industry circuit simulator like HSPICE or what have you, you would find that the offset would be exactly zero. Of course, where a real circuit fabricated out of real components, the offset would be close to zero, in fact." *Id*. at 231:16-232:6.

Arigna proposes to construe these terms to cover any adjustment "closer to zero," relying on the disclosures in the specification providing that "[t]he minimum offset is achieved when the output current from a current amplifier has reached a steady state; therefore it is substantially constant, ideally zero." '082 patent at 2:3-6. In a specific embodiment, the specification

describes the offset "regulated to a minimum and thereby to a constant value, ideally zero." *Id*. at 8:8-10. Arigna argues that these disclosures recognize that the claimed minimum does not need to be at or near zero—the only requirement is that the offset value is closer to zero. CRB at 27-28.

Staff agrees with Arigna that these terms are not indefinite, finding reasonable certainty for this limitation in view of the claims and specification. SIB at 76-77. Staff proposes to construe these terms to mean "regulating an offset to at or near zero" based on the same disclosures in the specification cited by Arigna. *Id*. at 40-43. Staff highlights the disclosures in the specification describing the minimum value as "ideally zero." '082 patent at 2:3-6, 8:10-11; *see also id.* at 6:17-19 ("preferably . . . zero"). The specification also describes this minimum as a "negligible offset." *Id*. at 7:31-35. Staff argues that Arigna's construction would read the term "minimum" out of the claim language, requiring only a reduction without reaching the lowest value or near zero, as described in the specification. SIB at 42-43. At the hearing, Dr. Souri joined in Staff's criticism of Arigna's proposed construction, offering his opinion that it would rewrite the claim to be regulating towards a minimum rather than "to a minimum." Tr. (Souri) at 1185:13-24.

In consideration of the parties' arguments, the undersigned finds that the terms "regulate the offset to a minimum" and "regulating the offset to a minimum" are not indefinite and shall be construed to mean "regulating an offset to at or near zero." The specification describes the minimum to be "ideally zero" or "preferably to the value of zero." '082 patent at 2:3-6, 6:17-19. It further describes the minimum as providing "no or only a negligible offset." *See id.* at 7:31-35 (stating that in certain embodiments where "a regulation of the offset Ioff to a minimum is possible . . . no or only a negligible offset Ioff interferes with the output signal Io of the circuit").

These disclosures are sufficient to "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). As recognized by Dr. Sechen, circuits meeting this limitation would achieve an offset of exactly zero "at the schematic level" using "a standard industry circuit simulator," but in "a real circuit fabricated out of real components, the offset would be close to zero, in fact." Tr. (Sechen) at 231:16-232:6; *see also id.* at 233:1-8. Staff's construction, supported by the testimony of Dr. Sechen, recognizes the inherent manufacturing imperfections and real-world engineering tolerances that may prevent the offset from reaching precisely zero, while providing reasonable certainty and remaining true to the claim language and the specification. *See* SIB at 77; *cf. Pulse Electronics, Inc. v. U.D. Electronic Corp*., 860 Fed. Appx. 735, 739 (Fed. Cir. July 1, 2021) ("desired effect of changing direction by approximately 90 degrees" not indefinite where PTAB had found that "approximately 90 degrees" means "'near or equal to 90 degrees' (to account, e.g., for 'manufacturing tolerances')" and "desired effect" has "a clear and objective meaning: that the conductors curve or change direction by approximately 90 degrees").[6] Here, unlike the situation addressed by the Federal Circuit in *Berkheimer v. HP Inc.* (*see* RRB at 7-8), there is expert testimony providing guidance as to the meaning of this limitation. 881 F.3d 1360, 1363-64 (Fed. Cir. 2018) (finding no clear error in indefiniteness finding "in light of the

[6] Complainant's proposed construction ("a value closer to zero") appears disconnected from its underlying argument that a "minimum" must be a steady state or "substantially constant" value. . Complainant's arguments regarding "substantially constant value" do not appear in its proposed construction. *See also* SIB at 42-43. In addition, the only support cited by Complainant for its argument regarding "closer to zero" is the testimony of Dr. Sechen, who testified that the value should be "close" (not "closer") to zero in view of real-world engineering issues. *See* CIB at 20 (citing Tr. (Sechen) at 232:7-233:8). The testimony of Dr. Souri, Respondents' expert, regarding Staff's proposed construction is conclusory and does not address the issue of real-world tolerances, and thus fails to meet the clear and convincing standard for indefiniteness. For these reasons and those discussed above, Complainant's proposed construction and Respondents' indefiniteness argument are rejected.

evidence in this case" where patentee offered no expert testimony); Tr. (Sechen) at 231:16-233:8.

For these reasons, the proper construction of "regulate the offset to a minimum" and "regulating the offset to a minimum" is "regulating an offset to at or near zero." The evidence does not show clearly and convincingly that the term is indefinite.

D. Level of Ordinary Skill in the Art

In the *Markman* order, the level of ordinary skill in the art was found to be a bachelor's degree in electrical engineering or a similar field, and approximately two years of industry or academic experience designing or analyzing electronic circuits, including experience with amplifiers. Order No. 30 at 10-11.

E. Infringement

Arigna's infringement allegations for the '082 patent are based on Dr. Sechen's analysis of the Analog Devices AD8417 chip used in the Hella 48V Converter of certain Mercedes vehicles and the Analog Devices AD8418 chip used in the Bosch 48V Converter of certain Volkswagen vehicles and in the Bosch LEB450 Inverter of certain BMW vehicles. CIB at 22-24; Tr. (Sechen) at 167:24-170:17. There are no material differences between the AD8417 and AD8418 chips for the purposes of the infringement analysis. *See* CIB at 23; SIB at 44 n.10; Tr. at 170:18-23 (Sechen), 1086:17-1087:8 (Sinenian).

1. Claim 1

Arigna alleges that components in the AD8417 and AD8418 chips meet each of the limitations of claim 1 of the '082 patent. CIB at 24-49; CRB at 28-51. Respondents and Staff dispute infringement of the "current amplifier" limitation, as discussed below. *See* RIB at 22-41; RRB at 10-22; SIB at 44-55; SRB at 12-18. Respondents also dispute infringement of the

"output current" limitation, because there is no "current amplifier." RIB at 41-42. Respondents further dispute infringement of the limitation requiring regulation of an offset "to a minimum." *Id*. at 41.

a. "A circuit comprising"

There is no dispute that the AD8417 and AD8418 chips comprise circuits. CIB at 24-25. Dr. Sechen identifies schematics and datasheets describing the circuitry of the AD8417 and AD8418 chips. Tr. (Sechen) at 216:7-13, 218:10-13; CX-00594C (AD8418 schematic); CX-00627C (AD8417 schematic).

b. "a current amplifier"

Arigna relies on Dr. Sechen's identification of a "current amplifier" in the AD8417 and AD8418 chips. CIB at 25-34; Tr. (Sechen) at 174:23-198:15. Specifically, Dr. Sechen identifies a "current amplifier" that he testified includes a differential current within the [redacted] of the AD8418 as the input to the "current amplifier" and a current provided to the [redacted] block as the output of the "current amplifier." Tr. (Sechen) at 175:7-25. A "top-level schematic" for the accused chips is shown below:

CDX-001C-27; CX-00594C; CX-00627C; Tr. (Sechen) at 174:8-175:25. Within the [redacted] (shown in CDX-001C-29 below), Dr. Sechen states that the asserted input current is the result of converting the voltage signals at [redacted], which he identifies as [redacted] Tr. (Sechen) at 176:1-181:10. He submits that the conversion of voltage to current is performed by [redacted] within the [redacted]. *Id*. at 177:20-178:15, 180:20-181:10. Based on the voltage and resistance disclosed in the Analog Devices schematics, Dr. Sechen calculates that the [redacted] value would be [redacted]. *Id*. at 179:16-180:19.

CDX-001C-29; CX-00621C; CX-00657C. Dr. Sechen submits that an [redacted] and [redacted] convert [redacted] current to voltages [redacted] Tr. (Sechen) at 183:12-24 ("This amplifier symbol here converts, and its associated resistance up here converts this [redacted] current into the voltage difference [redacted]. So the first thing that happens here is that the conversion within the [redacted] of this differential current into a differential voltage [redacted]."). He compares this functionality in the [redacted] to a portion of the circuit depicted in Figure 2a of the '082 patent, which he calls a [redacted] where the input current Isig is converted to voltage by the transistors 111 and 112. *Id*. at 183:25-184:8; *see* CIB at 28-29.

The [redacted] signals are output from the [redacted] to the [redacted] which includes [redacted] and [redacted], where further processing results in voltage signals [redacted] and [redacted] Tr. (Sechen) at 184:9-186:2.

CDX-001C-33; CX-00596C. The [redacted] and [redacted] signals are input to [redacted] (shown below), which generates a [redacted] and [redacted] Tr. (Sechen) at 195:6-198:15. Dr. Sechen explains that [redacted] and [redacted] have [redacted] but where there is a [redacted] one value would be higher than [redacted] while the other would be lower than [redacted]. *Id*. at 196:8-198:6.

CDX-001C-35; CX-00596C. The [redacted] and [redacted] current outputs then go through a [redacted] before being sent to the [redacted]. Tr. (Sechen) at 198:16-199:15. Arigna argues that the [redacted] function similarly to the [redacted] in the current amplifier described in the '082 patent specification. CIB at 32-33; *see* Tr. (Sechen) at 160:19-164:25. Dr. Sechen testified that a portion of the [redacted] contains the "output of the current amplifier," which encompasses currents [redacted] "which correspond to the [redacted] that came out of the [redacted]." Tr. (Sechen) at 199:16-200:21; CDX-001C-38; CX-00604C.

Respondents argue that the AD8417 and AD8418 chips do not comprise a "current amplifier." RIB at 22-41; RRB at 10-22. The datasheets for the AD8147 and AD8418 chips describe these circuits as "current sense amplifiers," and Dr. Sinenian explains that this is a type of voltage amplifier (not current amplifier) that is used to measure current. Tr. (Sinenian) at 1041:10-1042:16; RDX-0005C.7; RX-1784; RX-1787. The inputs to the AD8147 and AD8418

chips are differential voltage [redacted] and the final output is a voltage [redacted] Tr. (Sinenian) at 1046:6-1047:2; RDX-0005C.11; RX-1791C; RX-1796C. Dr. Sinenian notes that the schematics for the AD8147 and AD8418 chips include explicit labels describing their voltage gain. Tr. (Sinenian) at 1046:6-1047:6; RDX-0005C.11; RX-1791C; RX-1796C.

Respondents further submit that no individual stage of the AD8147 and AD8418 chips is a current amplifier. RIB at 25-36. With respect to Dr. Sechen's identification of a portion of the AD8147 and AD8418 circuitry as a "current amplifier," Respondents argue that this infringement theory was not disclosed in Complainants' pre-hearing brief and was therefore waived. RIB at 37-38; RRB at 8-10. Addressing the substance of this infringement theory, Respondents submit that Dr. Sechen failed to identify an appropriate input current for the alleged "current amplifier." RIB at 37-39. Dr. Sinenian explains that the [redacted] current value identified by Dr. Sechen is not a current signal that is amplified—it is merely a byproduct of the voltage signal [redacted]. Tr. (Sinenian) at 1053:1-1054:10. Dr. Sinenian submits that the current identified by Dr. Sechen in the [redacted] largely flows out of the chip to [redacted]." *Id.* at 1053:25-1054:3. Respondents thus argue that this [redacted], which is not labeled in any schematic, is not converted to [redacted] voltage signals, as suggested by Dr. Sechen. RRB at 13. Dr. Sinenian submits that Dr. Sechen's analysis of the [redacted] schematic (CX-00621C) is incorrect, because the [redacted] on the right side of the schematic represents additional components of the AD8417 chip that are [redacted]. Tr. (Sinenian) at 1050:20 -1051:5; RDX-0005C.16; RRB at 14.[7] Respondents thus argue

[7] Respondents submit that the [redacted] identified on the [redacted] schematic corresponds to the [redacted] from the [redacted], which is an input to the [redacted]. RRB at 17-18 (citing Tr. (Sinenian) at 1046:15-19, 1050:20-25, 1063:19-1064:5; RDX-0005C.11, 16, 33; Tr. (Sinenian) at 1051:6-13; RDX-0005C.16).

that there is no [redacted] or [redacted] in the [redacted] that converts the alleged [redacted] current into a voltage signal. RRB at 14-17. Dr. Sinenian submits that there is no circuitry for converting a current signal to a voltage signal between Dr. Sechen's [redacted] and the [redacted] of the [redacted]—they are merely [redacted]. Tr. (Sinenian) at 1100:6-11. Because there are no transistors in the [redacted] that convert [redacted] from a current signal to a voltage signal, Respondents argue that there is no basis for identifying a [redacted] in the [redacted] that can be compared with components depicted in the '082 patent. RRB at 18-19. Respondents note that there is no description of such stages in the '082 patent specification, and the [redacted] described in the patent are not present anywhere in the [redacted]. *Id*.

Respondents further argue that the alleged [redacted] current value is not amplified by the circuitry identified by Dr. Sechen. RIB at 40-41; RRB at 19-20. Dr. Sinenian testified that there is no "causal link" between the [redacted] current identified by Dr. Sechen and the [redacted] output in the [redacted]. Tr. (Sinenian) at 1059:18-1060:9. Respondents note that Dr. Sechen failed to provide any testimony that explains how the [redacted] is amplified in the [redacted] and [redacted] current outputs. RRB at 20.

Staff agrees with Respondents that the AD8417 and AD8418 chips are current sense amplifiers rather than current amplifiers. SIB at 45-46. Staff also agrees with Respondents that the infringement theory presented at the hearing by Dr. Sechen is inconsistent with Arigna's pre-hearing brief. *Id*. at 46-47. Staff further agrees with Respondents that Dr. Sechen's infringement theory is flawed, because the [redacted] current is not amplified by the identified circuitry, there is no "transresistance" amplifier in the [redacted], and Dr. Sechen's identification of portions of the AD8417 and AD8418 chips is arbitrary and unsupported by any evidence. *Id*. at 48-55.

To illustrate the fact that the [redacted] current is not amplified to obtain the [redacted] and [redacted] currents, Staff cites Dr. Sechen's admission that when the [redacted] the [redacted] and [redacted] outputs will have a value of [redacted]. *See* SIB at 48; Tr. (Sechen) at 572:7-15, 575:1-6. Staff cites Dr. Sinenian's testimony that the [redacted] at the [redacted] and [redacted] outputs is a [redacted] that is [redacted]. *See* SIB at 49; Tr. (Sinenian) at 1109:15-1110:2. Staff submits that the current values of [redacted] and [redacted] are a function of the voltage signals [redacted] and [redacted] pointing to the circuitry in the [redacted] that defines a [redacted]. SIB at 49-50. Staff argues that Dr. Sechen's testimony regarding the "transresistance" amplifier in the [redacted] is vague and conclusory, and Staff agrees with Dr. Sinenian's analysis of this circuitry. *Id*. at 50-53. Staff characterizes Dr. Sechen's analysis of the [redacted] as arbitrary, because he draws an imaginary line that excludes a [redacted] with [redacted]. *Id*. at 54-55. Staff submits that there is no evidence, other than Dr. Sechen's conclusory testimony, to support Arigna's argument that [redacted] SRB at 14-16. Moreover, Staff argues that the "current amplifier" described in the specification of the '082 patent does not convert voltage signals to current signals—it uses pairs of transistors to form a structure called a "current mirror," and no similar structure has been identified by Arigna in the AD8417 and AD8418 chips. *Id*. at 16-18.

In reply, Arigna argues that infringement can be proven based on a portion of the AD8417 and AD8418 chips, as identified by Dr. Sechen. CRB at 29-34. Arigna disputes the arguments by Respondents and Staff that Dr. Sechen's testimony was outside the scope of its pre-hearing brief or Dr. Sechen's expert report. *Id*. at 36-41. Arigna submits that Dr. Sechen's

analysis of the "current amplifier" is largely undisputed and supports a finding of infringement. *Id*. at 41-51.

In consideration of the parties' arguments and the evidence presented at hearing, the undersigned agrees with Respondents and Staff that Arigna has failed to identify, by a preponderance of the evidence, a "current amplifier" in the AD8417 and AD8418 chips. The plain and ordinary meaning of "current amplifier" requires a device which can take an input current signal and amplify that signal to provide an amplified output current. *See* Tr. (Sinenian) at 1033:4-1038:15 and RDX-0005C.4; RX-1629.5; RX-1630.31; RIB at 19-21; SIB at 30 (current amplifier is "a circuit that takes a current input and outputs the same current but amplified (i.e., with some amount of gain applied)"); *id.* at 32 ("current output by a current amplifier is the same current signal as the input current but with a gain of one or more applied"); Tr. (Sechen) at 158:24-159:3 (a current amplifier "is an amplifier that receives an input current and outputs a current that is larger than the input current"); *id.* at 183:16-17 (characterizing asserted input of current amplifier as "current signals"). An amplifier's "gain" is a "multiplicative factor that's applied to the input signal amplitude to get the output signal amplitude." Tr. (Sinenian) at 1035:8-15; RDX-0005C.4. The undersigned finds that this limitation is not met because Arigna has failed to identify, by a preponderance of the evidence, a "current amplifier" in the accused products.

As an initial matter, the undersigned shall consider Arigna's infringement arguments based on Dr. Sechen's testimony at the hearing regarding the [redacted] and the alleged [redacted] or [redacted] stage of the [redacted]. Respondents and Staff argue that this infringement theory was not disclosed in Arigna's pre-hearing brief, but this objection should have been raised at the hearing when Dr. Sechen offered his testimony. *See*

RIB at 36-39, RRB at 8-10, SIB at 46-47, SRB at 12-14. Dr. Sechen's identification of the [redacted] was explicitly allowed pursuant to Order No. 46 (Mar. 31, 2022). Although the undersigned agrees with Respondents and Staff that Arigna's pre-hearing brief did not identify any [redacted] or [redacted] stage in the [redacted], Dr. Sechen's testimony at hearing explicitly referenced the alleged [redacted] in the Analog Devices schematics. *See* Tr. (Sechen) at 164:10-18, 183:25-184:8, 257:8-16. Respondents and Staff did not object to this testimony at the hearing and it is now part of the record—Arigna will not be precluded from relying on Dr. Sechen's testimony on this issue. *See* CRB at 37-39.

Moreover, Dr. Sechen's testimony is consistent with the disclosures in Arigna's pre-hearing brief identifying current flowing through the [redacted] as the relevant input current for the alleged "current amplifier." CPHB at 31-32. Dr. Sechen elaborated on Arigna's argument by comparing certain components in the AD8417 and AD8418 chips with stages depicted in the specification of the '082 patent—this is not a new infringement theory but an attempt to support Arigna's infringement allegations with expert opinion. To the extent that some of these opinions may have been outside the scope of Dr. Sechen's expert report, Respondents and Staff should have raised the appropriate objection at the hearing or moved to strike the testimony. The record is now closed, and the undersigned will not preclude Arigna from relying on the admitted testimony of its expert.[8]

[8] On May 13, 2022, Respondents filed a motion (1267-050) to strike Exhibits A-C to Arigna's reply post-hearing brief, which were attached to address Respondents' arguments regarding waiver. Arigna filed a response in opposition to the motion on May 25, 2022. Staff filed a response in support of the motion on May 25, 2022. In Arigna's response, Arigna confirms that it does not seek the admission of these exhibits as substantive evidence and agrees that these exhibits are not part of the evidentiary record. Moreover, the undersigned has rejected Respondents' and Staff's waiver arguments without considering the content of Arigna's exhibits. Accordingly, the exhibits to Arigna's reply post-hearing brief will not be considered

On the merits, however, the undersigned finds that Arigna has failed to show that the circuitry identified in the AD8417 and AD8418 chips is a current amplifier, as understood by one of ordinary skill in the art.

First, it is undisputed that the AD8417 and AD8418 chips, as a whole, are "current sense amplifiers" that amplify voltage signals, not current signals. *See* Tr. (Sinenian) at 1041:17-1042:8; RX-1784; RX-1787. Dr. Sechen's identification of a "current amplifier" relies on identifying a [redacted] in a manner analogous to certain structures of the '082 patent to create "overall a current amplifier." *See* CIB at 26; Tr. (Sechen) at 258:1-20, 160:19-164:25, 183:25-184:2.

Dr. Sechen has not, however, persuasively identified a [redacted] in the accused chips. There is no dispute that the inputs [redacted] and outputs [redacted] of the [redacted] are voltage signals, not current signals. *See* CX-00621C; Tr. (Sechen) at 176:14-18, 183:12-24; Tr. (Sinenian) at 1050:5-14. Dr. Sechen testified that a [redacted] in the [redacted] converts the input voltage to an [redacted], which Dr. Sechen identifies as the input to his alleged current amplifier. Tr. (Sechen) at 177:15-178:15. Dr. Sechen further testified that a [redacted] then converts that [redacted] current back into a voltage signal [redacted] by an [redacted] and

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part of the evidentiary record, and the motion is DENIED-IN-PART as moot with respect to Arigna's arguments regarding waiver of Dr. Sechen's '082 patent infringement theories. *See infra*, n.59 (addressing other arguments in the motion to strike).

[9] Dr. Sechen testified that a [redacted] (Tr. at 162:7-10) and a [redacted] (Tr. at 163:3-5).

[redacted] *Id.* at 183:12-24; CDX-001C-32; *see also id.* at 580:21-581:2 (interpreting [redacted] as output of the [redacted]). However, this interpretation of the [redacted] schematic is not supported a preponderance of the evidence. According to the testimony of Dr. Sinenian, the [redacted] on the right side of the schematic represents additional components of the AD8417 chip that are outside of the [redacted]. *Id.* (Sinenian) at 1050:20 -1051:5; RDX-0005C.16; RRB at 17; SIB at 53. Arigna has identified no specific circuitry in the [redacted] that converts [redacted] to voltage signals [redacted], or that he shows are similar to the transistors in the "transimpedance" stage of the current amplifier in the '082 patent specification (as identified by Dr. Sechen). *See* Tr. (Sechen) at 161:20- 162:10 (describing "transimpedance" stage in Fig. 2a of the '082 patent); *see also* Tr. (Sinenian) at 1092:9-1093:5 (describing transistors in Fig. 2a of the '082 patent); RRB at 18.[10] Dr. Sinenian testified, in rebuttal, that the connection between [redacted] and voltage outputs [redacted] is simply a wire, and there is no persuasive evidence that a wire can constitute a [redacted]. *See* Tr. (Sinenian) at 1100:8-10 ("there's a wire connecting [redacted]"); RRB at 16-17. Accordingly, the undersigned finds that Arigna has failed to identify, by a preponderance of the evidence, any [redacted] for the alleged current amplifier in the AD8417 and AD8418 chips.

In addition, the record does not support, by a preponderance of the evidence, Arigna's contention that the differential current value of [redacted] and [redacted] (the output of the alleged current amplifier) is amplified from [redacted] Dr. Sinenian testified that [redacted] is merely a

[10] The schematic for the [redacted] shows that it receives input voltage signals [redacted] and outputs [redacted] Tr. (Sinenian) at 1050:5-14. As discussed *supra*, Dr. Sechen testified that certain [redacted] convert voltage to current (Tr. at 177:15-178:15), not the other way around.

"byproduct or side effect of a voltage signal applied to a [redacted] due to Ohm's law,[11] and largely flows out of the chip at [redacted] rather than being propagated to other components for amplification. Tr. (Sinenian) at 1053:8-15; *id*. at 1053:25-1054:10; RDX-0005C.016; RIB at 38; SIB at 49. There is no specific argument or testimony provided by Arigna addressing Dr. Sinenian's testimony that [redacted] largely flows out of the chip in this manner. *See also* Tr. (Sinenian) at 1058:8-1059:1 ("[t]here's no causal relationship" between Sechen's alleged input current and output current).

Given these deficiencies in the evidence, Arigna has not shown, by a preponderance, that the "current amplifier" limitation is met in the accused products. Further consistent with this finding, the fact that Dr. Sechen's approach requires subdividing logical blocks of a schematic for a voltage amplifier to identify the alleged "current amplifier,"[12] as well as the lack of any designation on the schematic of the alleged input [redacted] for such a current amplifier,[13] indicate that the chip was not designed to provide a "current amplifier" as recognized by one of skill in the art. *See* SIB at 53-55; Tr. (Sechen) at 443:1-23 (one would not substitute "a voltage amplifier or a transconductance amplifier" for a current amplifier because 'the fundamental input and output characteristics of these amplifiers are incompatible with the environment in which a current amplifier operates"). For at least these reasons, Arigna has not shown by a

[11] Ohm's Law relates current, voltage, and impedance (or resistance) through the equation "V=IR." *See* Tr. (Sechen) at 400:6-12; RDX-0006C.9. In the context of discussing Ohm's law, Dr. Sechen acknowledged that voltage differences will produce current as a by-product if there is a conducting path. *See* Tr. (Sechen) at 400:6-401:8.

[12] *See* Tr. (Sechen) at 580:21-581:6 (only a portion of the [redacted] is part of the current amplifier).

[13] *See* SIB at 48 n. 14; CDX-001C.29; CX-00621C; CX-00657C.

preponderance of the evidence that the "current amplifier" limitation of claim 1 of the '082 patent is met.

c. "an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the "adjusting circuit" limitation of claim 1 of the '082 patent. CIB at 34-35. Dr. Sechen identifies an "adjusting circuit" in the [redacted] of the AD8417 and AD8418 chips. Tr. (Sechen) at 199:16-201:2.

[redacted]

CDX-001C-38; CX-00604C; CX-00645C. This [redacted] includes a [redacted] and [redacted]. Tr. (Sechen) at 200:22-201:14. Dr. Sechen explains that [redacted] are implemented to correct an offset in the currents [redacted] *Id.* at 201:15-202:21. Dr. Sinenian did not dispute that this "adjusting circuit" is present in the

AD8417 and AD8418 chips except to the extent that it requires a "current amplifier." *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that the AD8417 and AD8418 chips contain circuitry corresponding to the "adjusting circuit" limitation of claim 1 of the '082 patent, except for the "output current of the current amplifier," as discussed above.

d. "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the first "wherein" clause of claim 1 of the '082 patent. CIB at 36-37. As discussed above, Dr. Sechen identified a controlled current source in the [redacted] comprising [redacted]. Tr. (Sechen) at 201:3-14. He further explains that this controlled current source provides [redacted] to the alleged "current amplifier." *Id*. at 220:18-221:4, 222:3-223:15. He submits that the controlled current source is "connectable to the current amplifier" because there is a [redacted] of the alleged "current amplifier" through [redacted] *Id*. at 221:5-20. Dr. Sinenian did not dispute that this limitation is met except to the extent that it requires a "current amplifier." *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that the AD8417 and AD8418 chips contain "controlled current source" circuitry for "producing an output current" meeting the limitations of the first "wherein" clause of claim 1 of the '082 patent, except that there is no "current amplifier," as discussed above.

e. "wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the second "wherein" clause of claim 1 of the '082 patent. CIB at 37-39. Dr. Sechen identifies a regulation element for the [redacted] current that is connectable by a switching device to an input of the controlled current source. Tr. (Sechen) at 203:1-15.

[redacted]

CDX-001C-40; CX-00604C; CX-00645C. The control loop (shaded in red) is a [redacted] Tr. (Sechen) at 207:24-209:4. Dr. Sechen explains that the current flowing from the [redacted] is the [redacted]. *Id*. at 209:5-11. A similar regulation element of a control loop [redacted]. *Id*. at 209:12-212:16;

CDX-001C-41. Dr. Sinenian did not dispute that this limitation is met except to the extent that it requires a "current amplifier." *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that the AD8417 and AD8418 chips contain a "first switching device" connecting a current output to a controlled current source that forms a "regulation element of a control loop" meeting the limitations of the second "wherein" clause of claim 1 of the '082 patent, except that there is no "current amplifier," as discussed above.

f. "wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the third "wherein" clause of claim 1 of the '082 patent. CIB at 39-42. Dr. Sechen identifies [redacted] that operate as holding elements for the [redacted] Tr. (Sechen) at 213:5-214:24; CDX-001C-42; CX-00604C; CX-00645C. He explains that the [redacted] Tr. (Sechen) at 214:25-215:18; CDX-001C-43; CDX-001C-44. Dr. Sinenian did not dispute that this limitation is met except to the extent it requires a "current amplifier." *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that circuitry in the AD8417 and AD8418 chips form a "holding element" when a "first switching device" is disconnected, meeting the limitations of the third "wherein" clause of claim 1 of the '082 patent, except that there is no "current amplifier," as discussed above.

g. "wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the fourth "wherein" clause of claim 1 of the '082 patent. CIB at 42-45. As discussed above in the context of the "control loop" limitation, Dr. Sechen explains that current flowing from the [redacted] of the controlled current source will [redacted]. Tr. (Sechen) at 209:5-11; CDX-001C-40. A similar regulation element of a control loop [redacted] *Id*. at 209:12-212:16; CDX-001C-41. He offers his opinion that the correction would result in an [redacted] or a [redacted]." Tr. (Sechen) at 232:21-233:8. He explains that the [redacted] and the [redacted]. *Id*. at 234:6-21.

Respondents argue that Dr. Sechen's testimony regarding this limitation is conclusory and fails to meet Arigna's burden to prove infringement. RIB at 41. Respondents do not identify any contrary evidence regarding the identified correction currents, however, and Dr. Sinenian did not dispute Dr. Sechen's analysis of this limitation at the hearing. *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the evidence of record, the undersigned finds that Arigna has shown by a preponderance that the "controlled current source" in the AD8417 and AD8418 chips is configured to "regulate the offset to a minimum," meeting the limitations of the fourth "wherein" clause of claim 1 of the '082 patent.

h. "wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current"

Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for the final "wherein" clause of claim 1 of the '082 patent. CIB at 45-47. As discussed above in the context of the "holding element" limitation, Dr. Sechen explains that [redacted] operate as holding elements for the [redacted]. Tr. (Sechen) at 213:5-214:24; CDX-001C-42; CDX-001C-43. Dr. Sinenian did not dispute Dr. Sechen's analysis of this limitation. *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that the "controlled current source" in the AD8417 and AD8418 chips is configured to "hold the current value, associated with the minimum," meeting the limitations of the final "wherein" clause of claim 1 of the '082 patent.

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As discussed above, Arigna has not identified a "current amplifier" in the AD8417 and AD8418 chips, and accordingly, no accused products infringe claim 1 of the '082 patent.

2. Claim 13

Claim 13 of the '082 patent depends from claim 1, further requiring "a control circuit that is configured to control the first switching device and is connectable to a control terminal of the first switching device." Arigna relies on Dr. Sechen's analysis of the AD8417 and AD8418 chips for this claim limitation. CIB at 47-48. Dr. Sechen identifies control circuitry in the AD8417 and AD8418 chips that comprises [redacted] discussed above in the context of the "first switching device." Tr. (Sechen) at 238:21-239:18.

CDX-001C-66; CX-00604C; CX-00645C. Dr. Sinenian did not dispute Dr. Sechen's analysis of this limitation. *See* Tr. (Sinenian) at 1087:16-1088:13.

Based on the undisputed evidence of record, the undersigned finds that Arigna has shown that the AD8417 and AD8418 chips contain a "control circuit" meeting the limitations recited in claim 13 of the '082 patent.

As discussed above, however, Arigna has not shown that the AD8417 and AD8418 chips infringe claim 1 of the '082 patent, and accordingly, no accused products infringe claim 13 of the '082 patent.

3. Claim 17

Arigna alleges infringement of claim 17 relying on the same evidence discussed above for claim 1 and additional analysis from Dr. Sechen. CIB at 48-57; Tr. (Sechen) at 239:19-250:22. Respondents and Staff dispute infringement of the "current amplifier" limitation, as discussed above in the context of claim 1. *See* RIB at 22-42; RRB at 10-22; SIB at 44-55; SRB

at 12-18. Respondents further dispute infringement of the limitation in claim 17 requiring "regulating an offset to a minimum . . . when an input signal of the current amplifier has a constant value." RIB at 39-40; RRB at 22-23.

a. "A method for correcting an offset of an output current of a current amplifier of a circuit"

Arigna relies on Dr. Sechen's infringement analysis for claim 1 to meet the limitations of the preamble of claim 17. CIB at 49-50; Tr. (Sechen) at 240:11-241:5. Respondents and Staff dispute Arigna's identification of a "current amplifier" in the AD8417 and AD8418 chips. RIB at 22-41; RRB at 10-22; SIB at 44-55; SRB at 12-18.

For the reasons discussed above in the context of claim 1, the undersigned finds that the AD8417 and AD8418 chips perform a method for correcting an offset of an output current, but Arigna has failed to identify a "current amplifier" in the accused products.

b. "connecting a controlled current source to an output of the current amplifier via a first switching device to form a regulation element of a control loop"

Arigna relies on Dr. Sechen's infringement analysis for claim 1 to meet the limitations of the "connecting" limitation of claim 17. CIB at 50-51; Tr. (Sechen) at 241:6-13. For the reasons discussed above in the context of claim 1, the undersigned finds that the AD8417 and AD8418 chips contain circuitry meeting the "controlled current source," "first switching device," and "a regulation element of a control loop" limitations of claim 17 of the '082 patent, except that there is no "current amplifier."

c. "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element"

Arigna relies on Dr. Sechen's infringement analysis for claim 1 to meet the "regulating an offset to a minimum," "setting a current value of the output current of the controlled current source," and "the controlled current source acting as the regulation element" limitations of the "of claim 17. CIB at 51-52; Tr. (Sechen) at 241:14-20. Dr. Sechen offers further analysis of the AD8417 and AD8418 chips with respect to the limitation requiring that regulating an offset to a minimum occurs "when an input signal of the current amplifier has a constant value." Tr. (Sechen) at 242:25-250:22. Dr. Sechen identifies the [redacted] as the "input signal of the current amplifier." *Id*. at 243:21-248:2.

[redacted]

CDX-001C-74. He explains that [redacted] is an [redacted] and accordingly, its value will be constant when there is no difference between [redacted] which would be the case when [redacted]. *Id*.

Respondents argue that [redacted] cannot be the claimed "input signal" because it is a voltage signal, not a current signal. RIB at 39-40. Respondents further argue that the [redacted] is not input to the "current amplifier" identified by Dr. Sechen. RRB at 23-24. Staff agrees with Respondents that [redacted] is a voltage, not a current signal. SIB at 55-56.[14]

In consideration of the parties' arguments, the undersigned agrees with Respondents that the [redacted] identified by Dr. Sechen is not an "input signal of the current amplifier" for three distinct reasons. First, for the reasons discussed above in the context of claim 1, Arigna has failed to identify a "current amplifier" in the AD8417 and AD8418 chips. Second, as discussed above in the context of claim construction, the claimed "input signal of the current amplifier" must be a current signal, and there is no dispute that [redacted] is a voltage signal. Third, Arigna has not shown, by a preponderance of the evidence, that [redacted] is an input to the alleged "current amplifier" identified by Dr. Sechen wherein [redacted] is the input current. Rather, the [redacted] voltage appears to be generated within the portion of the [redacted] that Dr. Sechen has designated as internal to the current amplifier and at the same stage as the [redacted] voltages, which are allegedly converted from the [redacted] current. *See* RRB at 23-24; CX-00621C; Tr. (Sechen) at 582:6-9 (border of current amplifier begins "after the green blocks"); CDX-0001.32; CDX-0001C.74. If the [redacted] voltage is generated within the alleged "current amplifier," it cannot be

[14] Respondents also dispute whether Arigna has carried its burden to show that the offset is regulated to a minimum, but as discussed *supra* in the context of claim 1, Respondents' argument is not supported by any expert testimony or other record evidence.

"an input signal of the current amplifier" that meets the claim limitation. *See* RIB at 23-24. Arigna has not shown, by a preponderance of the evidence, that the "input signal of the current amplifier" limitation of claim 17 is met by the accused products.

d. "disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current"

Arigna relies on Dr. Sechen's infringement analysis for claim 1 to meet the limitations of the "disconnecting" limitation of claim 17. CIB at 56-57; Tr. (Sechen) at 241:23-242:24. For the reasons discussed above in the context of claim 1, the undersigned finds that the AD8417 and AD8418 chips contain circuitry meeting the "disconnecting" limitation of claim 17 of the '082 patent, except that there is no "current amplifier."

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Accordingly, no accused products infringe claim 17 of the '082 patent.

4. Claim 29

Claim 29 of the '082 patent depends from claim 17, further requiring "a control circuit that is configured to control the first switching device and is connectable to a control terminal of the first switching device." Arigna relies on Dr. Sechen's analysis for claim 13 to meet this claim limitation. CIB at 57. For the reasons discussed above in the context of claim 13, the undersigned finds that the AD8417 and AD8418 chips contain a "control circuit" meeting the limitations recited in claim 29 of the '082 patent. As discussed above, however, Arigna has not shown that the AD8417 and AD8418 chips infringe claim 17 of the '082 patent, and accordingly, no accused products infringe claim 29 of the '082 patent.

For the reasons discussed above, Arigna has not shown that any accused product infringes any asserted claim of the '082 patent.[15]

F. Domestic Industry—Technical prong

Arigna contends that Microchip's ATMXT336S and ATMXT540S touch controllers practice claims 1, 13, 17, and 29 of the '082 patent. CIB at 60-103. Dr. Sechen reviewed schematics and other Microchip documents to offer his opinion that the ATMXT336S and ATMXT540S practice the asserted claims. Tr. (Sechen) at 251:17-305:1. The Microchip schematics and source code were identified by Stephanus Duvenhage, a vice president at Microchip, at his deposition. *See* CIB at 60-62 (citing JX-00014C (Duvenhage Tr.) at 15:20-25, 17:1-10, 19:8-15, 25:9-28:24, 29:3-25, 180:14-24; CPX-005C; CPX-008C.

Respondents argue that the schematics produced by Microchip are incomplete and unreliable. RIB at 42-44; RRB at 25-26. In reply, Arigna submits that Dr. Duvenhage's unrebutted testimony is sufficient to establish that the Microchip schematics represent the [redacted] in the ATMXT336S and ATMXT540S chips. CRB at 58-59 (citing JX-00014C at 29:3-25). Dr. Duvenhage identified labels on certain schematics identifying the [redacted] and [redacted] JX-00014C (Duvenhage Tr.) at 182:16-20, 183:21-23. Staff agrees with Arigna that Dr. Duvenhage's testimony is sufficient to show the Microchip schematics represent the [redacted] in the ATMXT336S and ATMXT540S chips. SRB at 18.

[15] Claims 17 and 29 are method claims, and Arigna accuses Respondents of inducing infringement of these claims through their customers' normal and customary use of the accused vehicles. CIB at 58-59. Dr. Sechen explained that there are "no circumstances" under which the accused vehicles could be operated without performing the claimed method. Tr. (Sechen) at 250:3-22. There is no dispute with respect to this inducement evidence, but the undersigned finds that there is no induced infringement because there is no direct infringement.

In consideration of the parties' arguments and the evidence of record, the undersigned finds that it is more likely than not that the Microchip schematics represent the [redacted] in the ATMXT336S and ATMXT540S chips. *See* CRB at 58-59; SRB at 18-19; JX-00014C at 25:9-25, 26:9-23, 29:3-25, 182:16-20, 183:21-23.

Respondents have not offered any evidence disputing the substance of Dr. Sechen's limitation-by-limitation analysis of the domestic industry products, which is addressed below.[16]

1. Claim 1

Arigna relies on Dr. Sechen's analysis of the ATMXT336 and ATMXT540S schematics to show that the domestic industry products practice each limitation of claim 1 of the '082 patent. CIB at 63-76, 84-96.

a. "A circuit comprising"

Dr. Sechen analyzed the ATMXT336S and ATMXT540S chips comprising a current amplifier and adjusting circuit, as discussed below. Tr. (Sechen) at 254:2-302:17.

b. "a current amplifier"

Dr. Sechen identifies a current amplifier in the schematic for the ATMXT336S with [redacted] and [redacted] and [redacted] Tr. (Sechen) at 254:2-259:4; CPX-008C; CDX-001C.0702-.0708. He identifies a [redacted] and a [redacted] in the ATMXT336S that is similar to Figure 2a of the '082 patent. Tr. (Sechen) at 257:12-16, 258:1-8. Dr. Sechen further identifies a current amplifier in the ATMXT540S schematics, Tr. (Sechen) at 295:4-297:20. He submits that the current amplifier in the ATMXT540S operates the same as the current amplifier in the ATMXT336S. *Id*.

[16] Staff agrees with Arigna that the record evidence shows that the ATMXT336 and ATMXT540S chips practice claims 1, 13, 17, and 29 of the '082 patent. SIB at 56.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain a current amplifier.

c. "an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device"

Dr. Sechen identifies an adjusting circuit for correcting the [redacted] output of the current amplifier in the ATMXT336S. Tr. (Sechen) at 258:19-264:17; CDX-001C.0705. He identifies a controlled current source and a switching device within the adjusting circuit. Tr. (Sechen at 259:19-264:17. He identifies a similar adjusting circuit in the ATMXT540S, wherein the switching device has a [redacted]. Tr. (Sechen) at 297:6-300:18.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of claim 1 of the '082 patent.

d. "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier"

Dr. Sechen traces the output of the current amplifier in the ATMXT336S to the output of the controller current source [redacted] Tr. (Sechen) at 278:25-280:23. Similarly, he traces the output of the current amplifier in the ATMXT540S to the output of the controlled current source. Tr. (Sechen) at 298:23-300:18.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of the first "wherein" clause of claim 1.

e. "wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop"

Dr. Sechen identifies a regulation element of a control loop in the ATMXT336S by tracing the output current of the current amplifier through the first switching device to the controlled current source. Tr. (Sechen) at 281:6-285:11. With respect to the ATMXT504S, Dr. Sechen identifies an input of the controlled current source (brown-dashed line) that is connectable by the first switching device (yellow-lined box) to the output of the current amplifier (red line and box). Tr. (Sechen) 295:4-305:1.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of the second "wherein" clause of claim 1.

f. "wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element"

Dr. Sechen identifies a holding element in the ATMXT336S that is formed when the first switching element disconnects the controlled current source from the output of the current amplifier. Tr. (Sechen) at 285:13-286:24. He identifies a similar holding element in the ATMXT540S. *Id*. at 300:3-18.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of the third "wherein" clause of claim 1.

g. "wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current"

Dr. Sechen identifies the regulation element in the ATMXT336S wherein the controlled current source "provides the offset cancelling current up and through the two transistors" and "attaches back to the output of the current amplifier, thereby providing a control loop, which regulates or cancels the offset and does so stably." Tr. (Sechen) at 283:17-285:11; CDX-001C.0713. He explains that in the regulation phase, the current "will regulate the offset to, in fact, zero with ideal components at the schematic level. Tr. (Sechen) at 286:25-288:9. Dr. Sechen explains that the ATMXT540S operates "much like the 336S" in cancelling the offset of the current amplifier. *Id*. at 300:25-301:19.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of the fourth "wherein" clause of claim 1.

h. "wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current"

Dr. Sechen identifies a [redacted] in the controlled current source of the ATMXT336S that is configured to hold a charge that is associated with the offset of the output current. Tr. (Sechen) at 285:13-290:20. He identifies a similar "holding element" in the ATMXT540S. *Id*. at 300:25-301:19.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain an adjusting circuit meeting the limitations of the final "wherein" clause of claim 1.

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Accordingly, the undersigned finds that Arigna has shown that the ATMXT336S and ATMXT540S chips practice claim 1 of the '082 patent.

2. Claim 13

Dr. Sechen explains that the first switching device in the ATMXT336S can [redacted] "so there is control circuitry necessarily present in this 336S product, and it [redacted] Tr. (Sechen) 291:11-21. With respect to the ATMXT540S, Dr. Sechen identifies a [redacted] *Id*. at 302:18-303:9.

Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips contain a control circuit meeting the limitations of claim 13, and accordingly, Arigna has shown that these products practice claim 13.

3. Claim 17

Arigna submits that the ATMXT336S and ATMXT540S chips practice claim 17 for the same reasons discussed above for claim 1. CIB at 78-83, 97-102.

a. "A method for correcting an offset of an output current of a current amplifier of a circuit"

For claim 17, Arigna relies on Dr. Sechen's analysis for claim 1 describing a method for correcting an offset of an output current of a current amplifier in the ATMXT336S and ATMXT540S chips. CIB at 79, 98; Tr. (Sechen) at 292:1-14, 303:1-304:7. For the reasons discussed above in the context of claim 1, the undersigned finds that the ATMXT336S and ATMXT540S chips perform a method for correcting an offset of an output current of a current amplifier in accordance with the limitations of claim 17.

b. "connecting a controlled current source to an output of the current amplifier via a first switching device to form a regulation element of a control loop"

Arigna relies on Dr. Sechen's analysis for claim 1 describing the regulation element of a control loop in the ATMXT336S and ATMXT540S chips to meet the corresponding limitation in claim 17. CIB at 79-80, 98-99; Tr. (Sechen) at 292:1-14, 303:1-304:7. For the reasons discussed above in the context of claim 1, the undersigned finds that the ATMXT336S and ATMXT540S chips include a switching device to form a regulation element of a control loop meeting the limitations of the "connecting" step of claim 17.

c. "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element"

With respect to the "regulating an offset to a minimum" limitation of claim 17, Arigna relies on Dr. Sechen's analysis of claim 1 describing the "regulation element" in the ATMXT336S and ATMXT540S chips. CIB at 80-82, 99-101; Tr. (Sechen) at 292:1-14, 303:1-304:7. For the limitation requiring that the current value is set "when an input signal of the current amplifier has a constant value," Dr. Sechen explains that the identified regulation loop [redacted] Tr. (Sechen) at 292:24-293:21, 304:8-20. Based on this unrebutted evidence, the undersigned finds that the ATMXT336S and ATMXT540S chips regulate an offset to a minimum in accordance with the limitations of claim 17.

d. "disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current"

Arigna relies on Dr. Sechen's analysis for claim 1 describing the holding element in the ATMXT336S and ATMXT540S chips to meet the corresponding limitation in claim 17. CIB at 82-83, 101-02; Tr. (Sechen) at 292:1-14, 303:1-304:7. For the reasons discussed above in the context of claim 1, the undersigned finds that the ATMXT336S and ATMXT540S chips include a switching device to form a holding element meeting the limitations of the "disconnecting" step of claim 17.

Accordingly, the undersigned finds that Arigna has shown that the ATMXT336S and ATMXT540S chips practice claim 17 of the '082 patent.

4. Claim 29

Arigna relies on Dr. Sechen's analysis for claim 13 describing the control circuit in the ATMXT336S and ATMXT540S chips to meet the corresponding limitation in claim 29. CIB at 83, 102-03; Tr. (Sechen) at 294:13-295:3, 303:11-16. For the reasons discussed above in the context of claim 13, the undersigned finds that the ATMXT336S and ATMXT540S chips include a control circuit in accordance with the limitations of claim 29.

Accordingly, the undersigned finds that Arigna has shown that the ATMXT336S and ATMXT540S chips practice claim 29 of the '082 patent.

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For the reasons discussed above, the evidence shows by a preponderance that Arigna satisfies the technical prong of the domestic industry requirement.

G. Domestic Industry—Economic prong

With respect to the economic prong of the domestic industry requirement, Arigna relies on Microchip's U.S. investments in labor and capital devoted to the ATMXT336S and ATMXT540S chips. CIB at 219-28. These expenditures were analyzed by Arigna's economic expert, Gregory Smith. Tr. (Smith) at 620:8-641:5.

1. Identification and Allocation of Expenditures

Mr. Smith reviewed Microchip's expenditures for maXTouch products starting in [redacted], the first full year after [redacted] Tr. (Smith) at 638:17-23; *see* JX-00014C (Duvenhage Tr.) at 41:9-42:1. Microchip's Human Machine Interface Division ("HMID") oversees the maXTouch product line, including the ATMXT540S and ATMXT336S chips. Tr. (Smith) at 624:3-5; JX-00014C (Duvenhage Tr.) at 18:3-15, 47:1-11. Mr. Smith estimates that HMID employees devoted to the maXTouch product line amounted to the equivalent of [redacted] each year from 2017 to 2020. Tr. (Smith) 638:4-11; CDX-002C.36. Certain maXTouch products are manufactured in Microchip's fabrication facility [redacted], [redacted] for the ATMXT540S and ATMXT336 chips. JX-00014C (Duvenhage Tr.) at 75:10-16. Mr. Smith also considered expenditures related to the maXTouch products in Microchip's [redacted] Tr. (Smith) at 632:10-18; *see* JX-00014C (Duvenhage Tr.) at 64:10-67:13. Arigna further identifies additional Microchip staff who perform work related to the maXTouch product line, including [redacted]

[redacted]

CIB at 222; JX-00014C (Duvenhage Tr.) at 68:8-25, 69:4-11, 70:24-72:20.

To allocate Microchip's expenditures to the ATMXT540S and ATMXT336S chips, Mr. Smith applies sales-based allocations. Tr. (Smith) at 626:20-627:6, 629:2-630:18; *see* CIB at 223-26. For HMID expenditures, he used the percentage of HMID global sales represented by the ATMXT540S and ATMXT336S chips to make the allocation. Tr. (Smith) at 629:19-630:1.

Revenue-Based Allocation: HMID

Detail	2017	2018	2019	2020	2021
082 DI Products Global Sales	[redacted]				
HMID Global Sales					
'082 DI Products % of HMID Business Unit					

CDX-002C.19 (citing CX-00061C; CX-00042C; CX-00039C). He applies these percentages directly to HMID salaries and benefits, totaling [redacted] from 2017-2021. Tr. (Smith) at 631:2-21; CDX-002C.24. He also applies these percentages to HMID direct operational expenditures, totaling [redacted] from 2017-020. Tr. (Smith) at 631:22-632:6; CDX-002C.26.

For TXFG expenditures, Mr. Smith used Microchip's percentage of global microcontroller sales represented by the ATMXT540S and ATMXT336S chips to make the allocation. Tr. (Smith) at 630:2-18.

Revenue-Based Allocation: Microcontroller

Detail	FY 2018	FY 2019	FY 2020	FY 2021
082 DI Products Global Sales	[redacted]			
Microcontroller Product Line Global Sales				
'082 DI Products % of Microcontroller Product Line				

CDX-002C.20 (citing CX-00061C; CX-00042C; CX-00563; CX-00477; CX-00440). He applies these percentages to TXFG salaries and benefits, totaling [redacted] from 2017-2021, and to TXFG direct operational expenditures, totaling [redacted] from 2017-2020. Tr. (Smith) at 632:10-633:2; CDX-002C.28; CDX-002C.30.

For wafer fabrication expenses, Mr. Smith used cost data for Microchip masks associated with the ATMXT336S (mask [redacted]) and ATMXT540S (mask [redacted]). Tr. (Smith) at 633:3-22. Because other devices are manufactured using mask [redacted], he used a revenue-based allocation to estimate the portion of wafer fabrication expenses for that mask that are attributable to the ATMXT336S. *Id.* The total estimated wafer fabrication expenses for the ATMXT336S and ATMXT50S from 2017-2020 was [redacted]. *Id.* at 634:20-635:6; CDX-004C.

Mr. Smith further allocated a portion of Microchip's global operating expenses to the ATMXT336S and ATMXT50S by applying an expense-based allocation to estimate the portion of these expenditures attributable to HMID and then applying the HMID revenue-based allocation discussed above, totaling [redacted] from 2017-2021. Tr. (Smith) at 633:23-634:14; CDX-002C.34.

The total estimated expenditures that Mr. Smith attributes to the ATMXT336S and ATMXT504S from 2017-2021 is [redacted]. Tr. (Smith) at 634:15-635:6.

Detail	2017	2018	2019	2020	2021	Total
HMID Salaries & Benefits	[redacted]					
HMID Direct Operational Expenses						
TXFG Salaries & Benefits						
TXFG Direct Operational Expenses						
Wafer Fabrication Expenses						
HMID Allocated Operating Expenses						
Total						[redacted]

CDX-004C.

Respondents argue that Arigna has failed to show that all of the identified expenditures qualify as part of a domestic industry and that Mr. Smith's allocations are unreliable. RIB at 181-84; RRB at 103-05. Respondents submit that the ATMXT540S and ATMXT336S were developed more than [redacted] years ago. RIB at 181 (citing Tr. (Smith) at 620:5-12). Respondents further submit that the ATMXT540S has generated [redacted] and that sales of the ATMXT336S have [redacted]. *See* RDX-0002C.5. Respondents argue that Arigna overstates the wafer fabrication expenses because the fabrication costs should have been allocated based on the unit sales in the following calendar year. RRB at 105; *see* RX-4239C. With respect to the Microchip labor costs allocated by Mr. Smith, Respondents argue that there is no evidence of any ongoing research and development, engineering, or technical services specific to the ATMXT540S or the ATMXT336S. RIB at 183-84; RRB at 103-04. Respondents submit that Mr. Smith was unable to identify [redacted] related to the ATMXT540S or the ATMXT336S in the 2017-2021

timeframe. RRB at 103-04. Respondents' expert, Brett Reed, offers an alternative estimate of domestic industry investments in labor and capital that totals [redacted] from 2017-2021. Tr. (Reed) at 951:12-952:3; RDX-0002C.7.

Staff supports Mr. Smith's allocation of expenditures, arguing that it was reasonable to employ a sales-based allocation where it is unlikely that Microchip tracks research and engineering activities on a product-by-product basis. SIB at 127; SRB at 53.

In consideration of the parties' arguments, the undersigned finds that Arigna has reliably quantified its domestic industry expenditures at least with respect to the wafer fabrication costs for the ATMXT540S and ATMXT336S chips. In particular, the undersigned finds Mr. Smith's calculation of [redacted] in wafer fabrication costs to be a reliable estimate of Microchip's wafer fabrication expenses between 2017 and 2020 at the [redacted] for the ATMXT540S and ATMXT336S chips. Tr. (Smith) at 634:20-635:6; CDX-004C.[17]

With respect to Mr. Smith's allocation of Microchip's HMID and TXFG expenditures, the undersigned agrees with Respondents that these estimates likely overstate the expenditures that can be fairly attributed to the ATMXT540S and ATMXT336S chips. Although the undersigned agrees with Staff that sales-based allocations can be a reliable way to estimate expenditures when there are no detailed accounting records, such allocations must be supported by evidence in the record that the methodology is appropriate to the circumstances. *See, e.g., Certain Mobile Device Holders and Components Thereof*, Inv. No. 337-TA-1028, Comm'n Op. at 18-19, EDIS Doc. ID 639588 (Mar. 22, 2018) (affirming an allocation using gross profits

[17] An alternative estimate produced by Mr. Reed also appears to use a reliable methodology, calculating total wafer fabrication expenditures of [redacted]—slightly less than Mr. Smith's estimate. *See* RRB at 105; RX-4239C. Mr. Reed did not provide any detailed testimony regarding this estimate at the hearing, however. *See* Tr. (Reed) at 952:12-953:2

where there was evidence that complainant "concentrates its resources researching and developing new technology and improvements where it can make the most profit."). Arigna fails to identify evidence in the record that sufficiently describes the activities of Microchip's HMID and TXFG employees with respect to the ATMXT540S and ATMXT336S chips and does not explain why it would be reasonable to allocate their salaries and benefits in accordance Microchip's global sales revenue for these products. Moreover, many of the identified groups of Microchip employees appear to [redacted]. *See* JX-00014C (Duvenhage) at 68:19-22 (describing the activities of Microchip's Marketing and Communications team). These activities should have been excluded from the domestic industry analysis. *See Certain Non-Volatile Memory Devices and Prods. Containing the Same*, Inv. No. 337-TA-1046, Initial Determination at 154-86, EDIS Doc. ID 646145 (Apr. 27, 2018) (categorizing "customer facing" engineering activities as sales and marketing), *aff'd* by Comm'n Op. at 44, EDIS Doc. ID 659979 (Oct. 26, 2018) ("The Commission has determined to affirm the ID's determination that Macronix failed to establish a domestic industry based on investments in 'customer facing' engineering for the reasons provided in the ID."). Mr. Smith made no attempt to separate sales and marketing activities from other domestic industry activities in his allocations.

Exclusion of Mr. Smith's allocations of Microchip's HMID and TXFG expenditures does not significantly affect the domestic industry analysis, however, because these expenditures represent a quantitatively small fraction of the asserted domestic industry in comparison to Microchip's wafer fabrication costs. *See* RIB at 181 (recognizing the [redacted] of the asserted domestic industry expenditures are wafer fabrication costs); SRB at 53-54 (recognizing that the difference between the expenditures recognized by Mr. Smith and Mr. Reed "is ultimately not

dispositive of the domestic industry analysis."). Moreover, Arigna does not rely on any of Microchip's labor expenditures to demonstrate the significance of the alleged domestic industry investments. *See infra.*

2. Significance

Arigna submits that Microchip's domestic industry expenditures are quantitatively and qualitatively significant. CIB at 227-28. Mr. Smith identifies several quantitative metrics, noting that the ATMXT540S and ATMXT336S account for [redacted] percent of the total revenue for the [redacted] line, although they only represent [redacted] percent of the products. Tr. (Smith) at 639:10-20. Mr. Smith calculated that the domestic wafer fabrication cost for the ATMXT336S ([redacted] per die) represents [redacted] of the average retail price ([redacted] per unit). Tr. (Smith) at 639:21-640:5; CDX-005C (citing CX-00061C; CX-00024C; CX-00056C). For the ATMXT540S, he calculated that the wafer fabrication cost ([redacted] per die) represents [redacted] of the average retail price ([redacted] per unit). *Id*. Arigna further argues that investing in maXTouch products is significant to the success of Microchip's business, including in the automotive sector. *See* JX-00014C (Duvenhage Tr.) at 44:10-45:11. Arigna also submits that Microchip's maXTouch products are likely to have a [redacted] and will be [redacted]. *See Id*. at 50:24-52:7.

Respondents argue that any expenditures related to the ATMXT540S are not significant because Microchip has not [redacted]. RIB at 181; *see* Tr. (Smith) at 669:21-670:3. Respondents submit that sales of the ATMXT336S [redacted] the ATMXT336S [redacted] any other Microchip products. RIB at 184; *see* Tr. (Reed) at 953:25-954:4. Respondents note that the ATMXT336S only accounts for a [redacted] of the wafer manufacturing in the "Fab 5" Colorado Springs

facility. *See* Tr. (Reed) at 954:5-15. Respondents also note that sales of the ATMXT336S represent a [redacted] of Microchip's total revenue, with a [redacted]. RIB at 184-85; *see* Tr. (Smith) at 674:16-21, 678:11-25. Respondents further argue that Arigna failed to account for foreign activities relating to the maXTouch product line, noting that Mr. Duvenhage testified that [redacted]. *See* JX-00014C (Duvenhage Tr.) at 82:6-10. All maXTouch products are [redacted], [redacted]. *See Id*. at 80:15-82:10, 134:5-23, 189:17-190:20.

Staff agrees with Respondents that Arigna cannot establish significance with respect to sales of the ATMXT504S chip, [redacted]. SIB at 127-28. Staff also agrees with Respondents that sales of the ATMXT336S do not appear to be significant within the context of the [redacted]. *Id*. Staff argues that Mr. Smith's comparison between wafer fabrication cost and average sales price does not show significance, because Arigna has not provided the total cost of manufacture, which would be necessary for a "value added" metric. *Id.* at 128-30; *see also* RRB at 106-07. Staff further contends that because the wafer fabrication costs include both labor and equipment costs, these expenditures cannot be aggregated under subsection (B) of section 337(a)(3). SIB at 130-31. Staff agrees with Respondents that the ATMXT540S and ATMXT336S chips do not appear to be significant to Microchip's business. *Id*. at 131-32.

In consideration of the parties' arguments, the undersigned finds that Microchip's investments in domestic wafer fabrication relating to the ATMXT336S chips are significant. The undersigned agrees with Respondents and Staff that Microchip's investments with respect to the ATMXT540S are not significant because Microchip has [redacted] ATMXT540S chips or

manufactured wafers for this product [redacted]. *See Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Comm'n Op. at 68, 2015 WL 6755093, at *36-39 (Oct. 30, 2015) (finding no domestic industry where complainant's investments with respect to the protected articles had ended before the complaint was filed). There is no dispute that Microchip has ongoing domestic investments with respect to the ATMXT336S chip, however, and Mr. Smith has provided analysis showing that Microchip's investment in the domestic fabrication of wafers is significant.

There is no dispute that all wafers for the ATMXT336S chip are manufactured in Microchip's [redacted]. Respondents point to evidence that a large number of wafers for Microchip's maXTouch products are manufactured abroad, but [redacted] testimony unequivocally confirmed that the ATMXT336S wafers are manufactured domestically. JX-00014C (Duvenhage Tr.) at 81:7-15. He testified that there were no plans to [redacted]. *Id*. at 77:5-8. He confirmed that "[t]he process that we use in [redacted], to my understanding," and "[t]he products we fabricate there, at this point, we cannot just [redacted]." *Id*. at 241:13-242:9.

The undersigned finds that Microchip's domestic investment is quantitatively significant based on Mr. Smith's calculation that the domestic wafer fabrication cost for the ATMXT336S ($0.44 per die) represents [redacted] of the average retail price ([redacted] per unit). Tr. (Smith) at 639:21-640:5; CDX-005C (citing CX-00061C; CX-00024C; CX-00056C); CIB at 228. The parties do not dispute the accuracy of Mr. Smith's calculation.[18] Staff argues that this percentage does not

[18] The [redacted] figure is corroborated by other data in the record regarding Microchip's wafer fabrication expenditures and revenue for the ATMXT336S. For example, a similar ratio can be calculated using

show significance, however, because it compares domestic expenditures to sales price, rather than overall manufacturing cost. SIB at 129-30. Although the undersigned agrees with Staff that a comparison of domestic expenditures to the overall cost of goods is the preferred "value-added" metric, the Commission has relied on comparisons between domestic investments and sales revenue in other investigations to find significance. *See, e.g., Certain Self-Anchoring Beverage Containers*, Inv. No. 337-TA-1092, Comm'n Op. at 13, EDIS Doc. ID 683010 (Jul. 24, 2019) (finding significance where, *inter alia*, "the evidence of record demonstrates that the amounts of investments in labor and capital are about 9 percent of the annual sales of the domestic industry product."); *Certain LED Lighting Devices and Components Thereof*, Inv. No. 337-TA-1107, Initial Determination at 36-37, EDIS Doc. ID 677813 (May 16, 2019) (finding significant investments in labor and capital based on a comparison of expenditures to revenues generated from sales), *not reviewed by* Comm'n Op. at 3, EDIS Doc. ID 687961 (Sept. 11, 2019). Moreover, a value-added calculation that compared the wafer fabrication cost to the total manufacturing cost—as suggested by Staff—would likely result in a higher percentage than the one computed by Mr. Smith, because the retail price would be expected to exceed the manufacturing cost.

Respondents' preferred methodology of comparing wafer fabrication expenditures to sales in the following calendar year. *See* RRB at 105; RX-4239C. According to Mr. Reed's estimates, Microchip spent [redacted] on wafer fabrication for the ATMXT336S in 2017, and if this corresponds to [redacted] in sales in 2018, then the domestic contribution is [redacted]. *See* RX-4239C; CDX-002C.19. Comparing 2018 wafer fabrication costs of [redacted] with 2019 sales of [redacted] results in a ratio of [redacted]; 2019 wafer fabrication costs of [redacted] with 2020 sales of [redacted] is a ratio of [redacted]; and 2020 wafer fabrication costs of [redacted] with 2021 sales of [redacted] is a ratio of [redacted]. *See* RX-4239C; CDX-002C.19. The overall ratio of total estimated wafer fabrication costs from 2017-2020 ([redacted]) to total sales of the ATMXT336S from 2018-2021 [redacted]) would be [redacted]. As discussed above, Respondents offered Mr. Reed's estimates for wafer fabrication costs into evidence and Staff does not contest Arigna's allocation of wafer fabrication costs, which were higher than Mr. Reed's. *See* RIB at 181-83; RRB at 105; SIB at 127; SRB at 53.

The undersigned further finds that Microchip's domestic wafer fabrication is qualitatively significant to the manufacture of the ATMXT336S chip. The Commission has found qualitative significance where a domestic industry is based on "core manufacturing activities," affirming an initial determination finding that "[s]uch activities have long been recognized as a domestic industry within the meaning of section 337." *Certain Toner Supply Containers and Components Thereof (II)*, Inv. No. 337-TA-1260, Comm'n Op. at 11-12, EDIS Doc. ID 777011 (Aug. 3, 2022). The evidence indicates that Microchip's domestic wafer fabrication is a critical part of the manufacturing process for the ATMXT336S chip that includes making the circuitry that practices the claims of the '082 patent. Mr. Duvenhage explained that the wafer fabrication requires [redacted] and [redacted] JX-00014C (Duvenhage Tr.) at 75:25-77:11. He also testified that [redacted] to my understanding." *Id*. at 241:13-242:1. The evidence thus shows that Microchip's domestic wafer fabrication is critical to the manufacture of the domestic industry product.

The undersigned agrees with Respondents and Staff that the volume of Microchip's sales (including the fact that sales of the ATMXT540S and ATMXT336S account for [redacted] percent of the total revenue for the maXTouch product line) does not demonstrate the significance of the domestic industry investments. The undersigned does not agree with Respondents, however, that the [redacted] of the ATMXT336S preclude Arigna from relying on investments in wafer fabrication for this product. *See* RIB at 185-86; RRB at 107. Respondents cite *Certain Integrated Circuits and Products Containing the Same*, where an Administrative Law Judge found that domestic industry investments were not significant where "the domestic

industry presently devoted to the [domestic industry product] is virtually defunct." Inv. No. 337-TA-1148, Initial Determination at 182-87, EDIS Doc. ID 712794 (May 22, 2020).[19] But Microchip's wafer fabrication for the ATMXT336S is [redacted]—the evidence does not show it is defunct. Moreover, the Commission has held that "[p]ast expenditures may be considered to support a DI claim as long as those investments pertain to the complainant's industry with respect to the articles protected by the asserted IP rights and the complainant is continuing to make qualifying investments at the time the complaint is filed." *Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, Comm'n Op. at 68, 2015 WL 6755093, at *36 (Oct. 30, 2015). Respondents and Staff do not dispute that Microchip has continued to make and sell the ATMXT336S up to the time of the complaint, and the [redacted] do not diminish the significance of Microchip's past investments. As discussed above, the undersigned's finding of significance is based on the proportion of the value of these products that is attributable to domestic wafer fabrication, not the volume of production.

Staff's argument that the wafer fabrication costs may include plant and equipment does not, under the circumstances here, change the significance analysis. *See* SIB at 130-31. The Commission has recognized that the three subsections of section 337(a)(3) "are listed in the disjunctive," and investments can, where appropriate, be counted under more than one subsection. *See Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097, Comm'n Op. at 7-8, EDIS Doc. ID 649139

[19] Respondents cite this determination as Commission precedent, but the Commission took no position on the economic prong of the domestic industry requirement on review of the initial determination. *See Certain Integrated Circuits and Products Containing the Same*, Inv. No. 337-TA-1148, Comm'n Op. at 14, EDIS Doc. ID 729178 (Dec. 30, 2020).

(Jun. 29, 2018) (finding that "research and development" expenditures are not limited to subsection (C) but may also be counted under subsections (A) and (B)). In the context of an economic prong analysis involving manufacturing costs under subsection (B), the Commission has permitted facilities rent and equipment expenditures to be considered when assessing significance. *See Certain Self-Anchoring Beverage Containers*, Inv. No. 337-TA-1092, Comm'n Op. at 13, EDIS Doc. ID 683010 (Jul. 24, 2019) ("[T]he evidence of record demonstrates that the amounts of investments in labor and capital are about 9 percent of the annual sales of the domestic industry product. In this regard, as to the employment of labor and capital, the ID allocated $245,000 (R&D salaries) to the '850 patent, and recognized the $237,600 (specifically, $84,000 (annual facility rent), $148,400 (equipment), and $5,200 (3D printing R&D equipment)) as employment of capital."); *id.* at 11-12 (noting the ID's inclusion of rent and equipment as employment of capital and finding the record evidence supported the ID's findings); *cf. Certain Toner Supply Containers and Components Thereof (II)*, Inv. No. 337-TA-1260, Comm'n Op., at 10-11 (Aug. 3, 2022) (EDIS Doc. ID 777011) (assessing quantitative significance under subsections (A) and (B) based on a comparison of "domestic plant and equipment and labor and capital values to total market value").[20, 21]

For the reasons discussed above, the undersigned finds that Arigna has satisfied the economic prong of the domestic industry requirement based on Microchip's significant employment of labor and capital in domestic wafer fabrication for the ATMXT336S chip.

[20] *See also* 26 C.F.R. § 1.150-1(b) ("Capital expenditure means any cost of a type that is properly chargeable to capital account . . . For example, costs incurred to acquire, construct, or improve land, buildings, and equipment generally are capital expenditures.").

[21] Even if Microchip's plant and equipment expenditures were excluded, a preponderance of the evidence indicates that this would not affect the determination of significance, because Mr. Smith testified that wafer fabrication cost only includes "a small amount of depreciation of building and equipment." Tr. (Smith) at 704:24-705:3; *see also id*. at 705:14-17.

H. Invalidity

Respondents contend that the asserted claims of the '082 patent are invalid as anticipated or obvious in view of certain prior art references. RIB at 44-92. In particular, Respondents rely on Japanese Patent Publication No. S62-171212 to Soneda (RX-2096, "Soneda"), *A CMOS Low-Noise and Low-Power Charge Sampling Integrated Circuit for Capacitive Detector/Sensor Interfaces* by Suharli Tedja, *et al.*, IEEE Journal of Solid-State Circuits, vol. 30, No. 2 (Feb. 1995) (RX-1238, "Tedja"), and U.S. Patent No. 6,094,246 to Kozisek *et al.*, (RX-2080, "Kozisek"). Respondents' invalidity contentions are supported by the expert testimony of Dr. Shoukri Souri. *See* Tr. (Souri) at 1112:2-1221:7. Arigna disputes certain of Respondents' invalidity contentions, relying on the testimony of Dr. Sechen. *See* Tr. (Sechen) at 1243:4-1284:18.

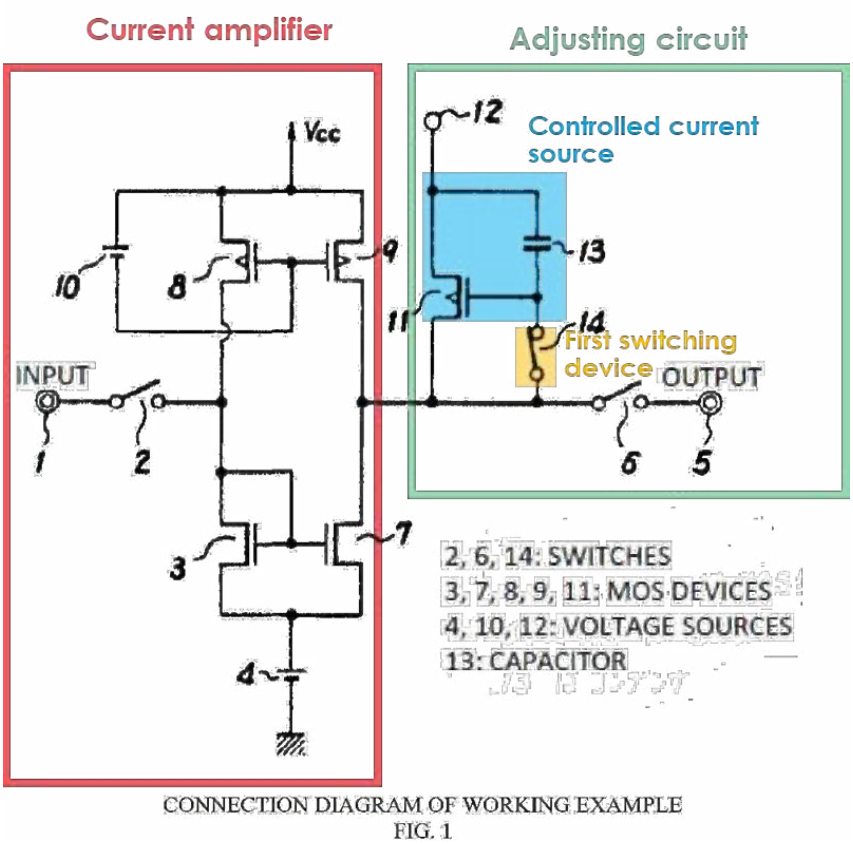
1. Anticipation by Soneda (Claim 1 and 17)

Soneda is an unexamined patent application from the Japanese Patent Office published on July 28, 1987, which is prior art to the '082 patent. RX-2096. Respondents contend that Soneda anticipates claims 1 and 17 of the '082 patent. RIB at 45-57; RRB at 27-29; Tr. (Souri) at 1126:16-1127:2. Arigna argues that Soneda does not anticipate any claim because it fails to disclose the claimed "regulation element of a control loop." CIB at 103-107; CRB at 62-67; Tr. (Sechen) at 1244:11-1246:18. Staff agrees with Respondents that Soneda anticipates claims 1 and 17 of the '082 patent. SIB at 57-63; SRB at 19-21.

a. Claim 1

i. "A circuit comprising"

Dr. Souri identifies circuit diagrams in Soneda describing a "current amplifier" and an "adjusting circuit." Tr. (Souri) at 1138:5-1140:8.



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

RDX-0001C.60 (annotating RX-2096, Fig. 1). Based on this unrebutted evidence, the undersigned finds that Soneda discloses a circuit.

ii. "a current amplifier"

Dr. Souri identifies a current amplifier in Soneda that includes a pair of transistors arranged to form a current mirror. Tr. (Souri) at 1139:4-23; RDX-0001C.59; *see* RX-2096 at 3-4 (describing prior art current amplifier depicted in Fig. 5), 5-6 (describing current amplifier of Fig. 1). Based on this unrebutted evidence, the undersigned finds that Soneda discloses a current amplifier.

iii. "an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device"

Dr. Souri identifies an adjusting circuit in Soneda that includes a controlled current source and first switching device that is configured to correct an offset from the current amplifier. Tr. (Souri) at 1139:24-1140:8; RDX-0001C.60; *see* RX-2096 at 5 ("[T]he source of this device (11) is connected to a voltage source (terminal) (12), a capacitor (13) is provided between the source and the gate of this device (11), and a switch (14) is provided between the drain and the gate of the device."), 6 ("[A]ccording to this circuit, a current that is equal to the offset current ΔI_{DC} is supplied from the device (11) in the operation interval Φ_E."). Based on this unrebutted evidence, the undersigned finds that Soneda discloses the components recited in the "adjusting circuit" limitation of claim 1 of the '082 patent.

iv. "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier"

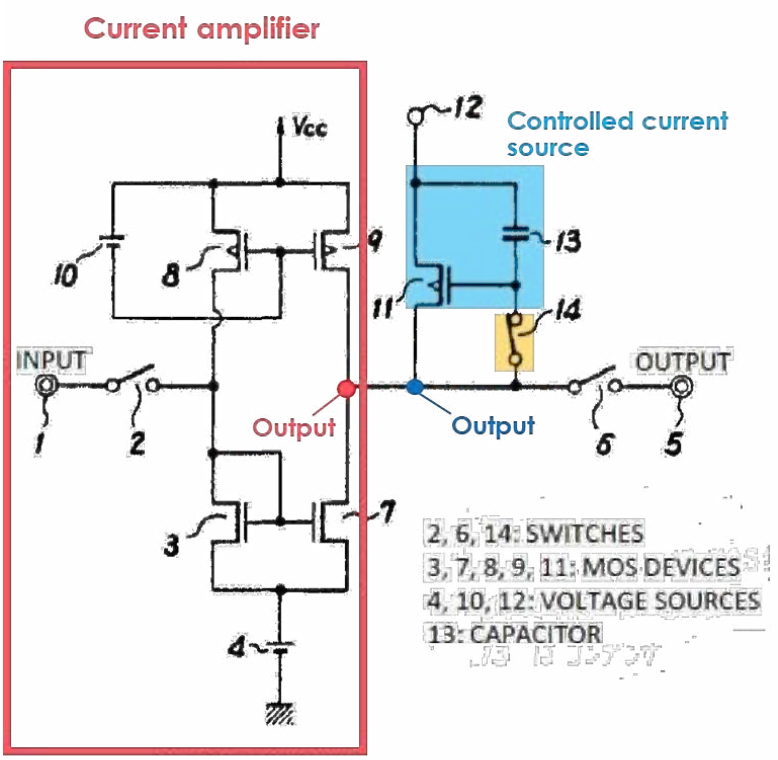
Dr. Souri identifies a connection between Soneda's current amplifier and the controlled current source of the adjusting circuit that allows the output of the controlled current source to be produced in the current amplifier. Tr. (Souri) at 1140:9-1141:9; RDX-0001C.61; *see* RX-2096 at 5 ("[T]he drain of a P-type MOS device (11) is connected to a connection midpoint between the devices (7) (9) and the switch (6)."); RIB at 49-50.[22] Based on this unrebutted evidence, the

[22] Dr. Souri further explains how this structure is similar to an alternative embodiment disclosed in the specification of the '082 patent where the output of the controlled current source is connected directly to the output of the current amplifier. Tr. (Souri) at 1141:12-1142:2; RDX-0001C.62; *see also* Tr. (Souri) at 1124:24-1125:10; RDX-0001C.15.

undersigned finds that Soneda discloses an adjusting circuit meeting the limitations of the first "wherein" clause of claim 1 of the '082 patent.

v. "wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop"

Dr. Souri identifies a "control loop" in Soneda that "is essentially a logical construct that results in feedback, information being fed back to the transistor 11 through charge and voltage that is developed on capacitor 13 to result in the cancellation of the offset current." Tr. (Souri) at 1151:11-52:3. He explains that a regulation element of the control loop is formed when switch 14 is closed. *Id*. at 1150:24-1153:6; *id.* at 1152:8-13 ("When switch 14 closes in Soneda, it connects the output of . . . the current amplifier to the input of the controlled current source, thereby information about this offset current is being delivered to the adjusting circuit forming that control loop.").



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

RDX-0001C.63-64; RX-2096 at 6 (when "the switch (14) is turned ON in a blanking interval Φ_B, an offset current Δ_{DC} at this time flows through the device (11) and, furthermore, the capacitor (13) is charged as this current flows"). Dr. Souri compares Soneda's control loop with a disclosure in the specification of the '082 patent where the capacitor 212 and transistor 213 form a similar structure when switch S1 is closed. Tr. (Souri) at 1152:18-1153:6; RDX-0001C.64.

Arigna argues that there is no "regulation element of a control loop" disclosed in Soneda. CIB at 103-07. In particular, Dr. Sechen explains that there is no "control loop" associated with the "regulation element" of Soneda: "[D]uring regulation, the current flows from node 12 through the blue, transistor 11, straight through to transistor 7. And there's no loop. It's just a current path from the supply at 12 to ground." Tr. (Sechen) at 1245:11-14. He describes this arrangement as "a diode connected transistor" rather than a "control loop." *Id.* at 1245:3-10.

Dr. Sechen submits that a regulation element as disclosed in Soneda would not correct the current offset as claimed in the '082 patent—Dr. Sechen suggests that without the control loop depicted in Figure 2a of the '082 patent, the "voltage will vary and the output current [is] very sensitive to this voltage. So the offset of the current amplifier is going to change during the holding period. And the offset you arrived at, at the end of the regulation period is no longer proper." *Id*. at 1246:19-1247:12.

Respondents argue that the '082 patent discloses an alternative embodiment with a control loop that is similar to the configuration disclosed in Soneda, where the controlled current source is connected directly to the output of the current amplifier. RIB at 53; *see* '082 patent at 3:62-63 ("Preferably, the controlled current source is connected to the output of the current amplifier directly or via a component."), 6:52-54 ("It would also be possible to connect controlled current source 210 directly to output 102 of input amplifier 100."). Respondents argue that the "control loop" limitation of the '082 patent does not require current to physically flow in a loop, citing Dr. Sechen's admission that the claimed "control loop" is a signal loop that is a logical construct rather than a physical construct. Tr. (Sechen) at 1273:1-18. And Respondents criticize Dr. Sechen's criticism of a direct connection configuration as conclusory and unsupported testimony. RRB at 28-29. Staff agrees with Respondents that Soneda discloses a "control loop." SIB at 59-62; SRB at 19-21.

In consideration of the parties' arguments, the undersigned finds that there is clear and convincing evidence that Soneda discloses a "control loop" meeting the limitations of the second "wherein" clause of claim 1 of the '082 patent. The evidence shows that the claimed "regulation element of a control loop" does not require a physical loop of current, but rather a signal loop which allows for the current offset to be corrected. *See* Tr. (Souri) at 1151:20-1152:3 (control

loop is "essentially a logical construct that results in feedback"); Tr. (Sechen) at 1273:1-18 (control loop is a "logical construct or "signal loop," not a current path).[23] Soneda discloses that, when switch (14) is turned on during the "blanking interval," "an offset current Δ_{DC} at this time flows through the device (11) and, furthermore, the capacitor (13) is charged as this current flows." RX-2096 at 6. Soneda further discloses that, as a result, when switch (14) is turned off, "the device (11) is biased by the charging electric potential of the capacitor (13)" and "a current that is equal to the offset current ΔI_{DC} is supplied from the device (11) in the operation interval Φ_E, and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current ΔI_{DC}." *Id*. Dr. Souri testified that the interaction of these structures (the switch, transistor, and capacitor) meet the "control loop" limitation of the '082 patent. Tr. (Souri) at 1151:20-1152:3; *id.* at 1128:22-1129:4. Dr. Souri further testified that the "control loop" disclosed in Figure 2a of the '082 patent operates in a similar manner to Soneda utilizing the "same three components." Tr. (Souri) at 1152:18-1153:6; RDX-0001C.64.

Dr. Sechen's contrary opinion that the asserted control loop in Soneda does not read onto the "control loop" limitation is based on his view that the Soneda structure is not a "loop" but "just a current path . . . to ground." Tr. (Sechen) at 1245:3-17. On cross-examination, however, he admitted that a "control loop" does not require a physical loop of current. Tr. (Sechen) at 1273:1-18. Arigna further argues that an "alternative embodiment" of the '082 patent, which Dr.

[23] Dr. Sechen's argument that a "regulation element of a control loop" necessarily requires a "cause/effect loop possibly translating or normally translating from voltages to currents, possibly back to voltages, that creates a negative feedback loop, which means . . . if you have a perturbation . . . and as you traverse or make one traversal around the loop in the circuitry, when you come back to where you started, that perturbation will be reduced. And additional perturbations will also reduce that to at or near zero" (Tr. (Sechen) at 1244:11-21)) lacks support in the record. *See* SIB at 59; SRB at 19. Arigna did not propose this term for construction and the evidence fails to persuasively show that one of ordinary skill in the art would limit the term "regulation element of a control loop" to such a structure.

Souri compared to Soneda's disclosure,[24] would not work. CIB at 106 (citing Tr. (Sechen) at 1247:13-1248:10 (discussing RDX-0001.15)[25]). However, Dr. Sechen's unsupported testimony that the "alternative embodiment" would not work contradicts the '082 patent. *See* Tr. (Souri) at 1124:24-1125:13; RDX-0001C.15; '082 patent at 3:62-63 ("Preferably, the controlled current source is connected to the output of the current amplifier directly or via a component."); *cf. Ericsson Inc. v. Intellectual Ventures I, LLC*, 890 F.3d 1336, 1346 (Fed. Cir. 2018) ("To contradict a reference, an unsupported opinion is not substantial evidence."); RIB at 53; RRB at 28-29.[26]

Accordingly, the undersigned finds that Soneda discloses, by clear and convincing evidence, an adjusting circuit meeting the limitations of the second "wherein" clause of claim 1 of the '082 patent.

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[24] Tr. (Souri) at 1141:12-1142:2; RDX-0001C.62; *see also* Tr. (Souri) at 1124:24-1125:10; RDX-0001C.15.

[25] Although the hearing testimony refers to slide 16, it is clear that slide 15 was intended.

[26] In addition, as discussed *infra*, Dr. Sechen also testifies that Kozisek's adjusting circuit is "substantially the same" as Soneda's. Tr. (Sechen) at 1262:12-1263:17. Arigna's argument that the adjusting circuit in Soneda would not work to correct the offset current (CRB at 66) thus implies that neither the circuit taught by Soneda nor the circuit taught by Kozisek would cancel the offset current as disclosed in each of these references. *See* RX-2096 at 6; Tr. (Souri) at 1151:11-1152:1, 1153:7-1154:24; RDX-0001C.66; RX-2080 at 6:16-53; Tr. (Souri) at 1178:10-1180:20; RDX-0001C.103, 107. Dr. Sechen's unsupported testimony is inadequate to make this showing, which would require Arigna to overcome a presumption that the prior art references are enabling. *See Impax Lab'ys, Inc. v. Aventis Pharms., Inc.*, 545 F.3d 1312, 1316 (Fed. Cir. 2008) (requiring "persuasive" evidence to overcome "a presumption that the anticipating disclosure also enables the claimed invention" in context of prior art patent); *In re Antor Media Corp.*, 689 F.3d 1282, 1287-89 (Fed. Cir. 2012) (extending this presumption to prior art printed publications in context of prosecution); *Apple Inc. v. Corephotonics, Ltd*., 861 Fed. Appx. 443, 450 (Fed. Cir. June 23, 2021) ("We do not see a principled distinction between our cases holding that this presumption and burden apply during patent examination and in district court litigation, and AIA trial proceedings. Thus, regardless of the forum, prior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art."); *Process Control Corp. v. HydReclaim Corp*., 190 F.3d 1350, 1359 (Fed. Cir. 1999) (inoperability implicates enablement requirement).

vi. "wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element"

Dr. Souri identifies Soneda's disclosure of a holding element formed when switch 14 opens and "the electric potential remains, on capacitor 13, continuing to bias transistor 11 and thereby canceling the offset current." Tr. (Souri) at 1153:7-25; RDX-0001C.65; *see* RX-2096 at 6 ("Furthermore, when the switch (14) is turned OFF in an operation interval Φ_E, the device (11) is biased by the charging electric potential of the capacitor (13)."). Based on this unrebutted evidence, the undersigned finds that Soneda discloses an adjusting circuit meeting the limitations of the third "wherein" clause of claim 1 of the '082 patent.

vii. "wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current"

As discussed above in the context of the second "wherein" clause, Dr. Souri identifies a control loop disclosed in Soneda, wherein in the capacitor 13 and transistor 11 output current that is equal to the offset of the current amplifier to cancel the offset. Tr. (Souri) at 1154:1-12; RDX-0001C.66; *see* RX-2096 at 6 ("[A]ccording to this circuit, a current that is equal to the offset current ΔI_{DC} is supplied from the device (11) in the operation interval Φ_E, and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current ΔI_{DC}.").

For the same reasons discussed above in the context of the second "wherein" clause, the undersigned finds that Soneda discloses an adjusting circuit meeting the limitations of the fourth "wherein" clause of claim 1 of the '082 patent.

viii. "wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current"

As discussed above in the context of the third "wherein" clause, Dr. Souri identifies a holding element disclosed in Soneda, wherein the capacitor 13 holds the charge necessary for producing a current to cancel the offset. Tr. (Souri) at 1154:13-24; RDX-0001C.67; *see* RX-2096 at 6 ("[T]he device (11) is biased by the charging electric potential of the capacitor (13), and a current ΔI_{DC} continues to flow between the source and the drain of the device (11)."). Based on this unrebutted evidence, the undersigned finds that Soneda discloses an adjusting circuit meeting the limitations of the final "wherein" clause of claim 1 of the '082 patent.

Accordingly, the undersigned finds that Soneda anticipates claim 1 of the '082 patent.

b. Claim 17

Respondents contend that Soneda anticipates claim 17 of the '082 patent for many of the same reasons discussed above for claim 1. RIB at 56-57; *see* Tr. (Souri) at 1155:17-1157:5.

i. "A method for correcting an offset of an output current of a current amplifier of a circuit"

As discussed above in the context of claim 1, Dr. Souri explains how the circuit disclosed in Soneda corrects the offset of a current amplifier. *See* Tr. (Souri) at 1154:1-12; RX-2096 at 6 ("[A]ccording to this circuit, a current that is equal to the offset current ΔI_{DC} is supplied from the device (11) in the operation interval Φ_E, and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current ΔI_{DC}."). Based on this unrebutted evidence, the undersigned finds that Soneda discloses a method meeting the preamble limitations of claim 17 of the '082 patent.

ii. "connecting a controlled current source to an output of the current amplifier via a first switching device to form a regulation element of a control loop"

As discussed above in the context of claim 1, Dr. Souri identifies a regulation element of a control loop disclosed in Soneda that is formed when switch 14 is closed. *See* Tr. (Souri) at 1150:24-1153:6; *see* RX-2096 at 6 ("[A]ccording to this circuit, a current that is equal to the offset current ΔI_{DC} is supplied from the device (11) in the operation interval Φ_E, and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current ΔI_{DC}."). For the same reasons discussed above in the context of claim 1, the undersigned finds that Soneda discloses the use of a switching device to form a regulation element of a control loop that meets the limitations of the "connecting" step of claim 17 of the '082 patent.

iii. "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element"

Dr. Souri explains that Soneda's regulation phase occurs when switch (2) is open and there is "no input signal or zero input signal, and zero is a constant value." Tr. (Souri) at 1155:25-1156:12; RDX-0001C.70; *see* RX-2096 at 6 ("[W]hen switches (2) (6) are turned OFF and the switch (14) is turned ON in a blanking interval Φ_B, an offset current ΔI_{DC} at this time flows through the device (11) and, furthermore, the capacitor (13) is charged as this current flows."). Based on this unrebutted evidence and for the same reasons discussed above in the context of claim 1, the undersigned finds that Soneda discloses setting a current value when the input signal of the current amplifier has a constant value meeting the limitations of the "regulating" step of claim 17 of the '082 patent.

iv. "disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current"

As discussed above in the context of claim 1, Dr. Souri identifies a holding element disclosed in Soneda that is formed when switch 14 is open. *See* Tr. (Souri) at 1153:7-25; *see* RX-2096 at 6 ("Furthermore, when the switch (14) is turned OFF in an operation interval Φ_E, the device (11) is biased by the charging electric potential of the capacitor (13)."). Based on this unrebutted evidence, the undersigned finds that Soneda discloses the use of a switching device to form a holding element that meets the limitations of the "disconnecting" step of claim 17 of the '082 patent.

Accordingly, the undersigned finds that Soneda anticipates claim 1 and claim 17 of the '082 patent.

2. Obviousness Based on Soneda in View of Kozisek (Claims 13 and 29)

Claims 13 and 29 of the '082 patent are dependent claims that add limitations to the independent claims 1 and 17 requiring "a control circuit that is configured to control the first switching device and is connectable to a control terminal of the first switching device."

Respondents contend that claims 13 and 29 are rendered obvious by Soneda in view of Kozisek, a U.S. Patent entitled "Amplifier Offset Cancellation Using Current Copier." RIB at 58-59 (citing RX-2080). Kozisek issued on April 11, 2000, which is prior art to the '082 patent. RX-2080. Staff agrees with Respondents that claim 13 is rendered obvious by Soneda in view of Kozisek. *See* SIB at 64-65; SRB at 23-24.

With respect to the added limitations of claims 13 and 29, Dr. Souri identifies control blocks disclosed in Kozisek controlling switches in an adjusting circuit. Tr. (Souri) at 1137:18-1138:4; RDX-0001C.54. Kozisek describes "a control circuit for selecting between a

cancellation mode and an operating mode." RX-2080 at 3:19-22. In a specific embodiment, Kozisek identifies "Switch Control C" in block 112, which controls "N-channel transistor 134" corresponding to switch 70. RX-2080 at 8:26-37. RDX-0001C.113 (citing RX-2080, Fig. 5).

Dr. Souri identifies disclosures in Soneda describing the precise timing of its switches during blanking interval Φ_B and operation interval Φ_E. Tr. (Souri) at 1157:8-24; RDX-0001C.71. Dr. Souri points to the disclosures in Kozisek discussed above describing control circuits providing signals to control switches corresponding to different modes of operation. Tr. (Souri) at 1157:25-1158:7. He explains that the requirements of Soneda's switches would motivate one of ordinary skill in the art to implement control circuitry like the controls disclosed in Kozisek. *Id*. at 1158:8-21. He explains that these are commonly known elements that a person of ordinary skill could implement with a reasonable expectation of success. *Id*. at 1158:22-1159:8.

Arigna does not specifically dispute Respondents' obviousness arguments based on combining Soneda (for purposes of all claim limitations in claims 1 and 17) with Kozisek (for purposes of the added "control circuit" limitations of claims 13 and 29). *See* CIB at 111-116; CRB at 76-77; SRB at 23-24. Arigna's arguments regarding the lack of motivation to combine are directed towards combining the adjusting circuit of Kozisek with the amplifier of Soneda or Tedja, not the different combination at issue here, which involves use of a control circuit to control a switching device. *See* CIB at 111; CRB at 71-74; SRB at 23-24.[27]

To the extent Arigna argues that there can be no motivation to combine information in the references simply because Soneda discloses a current amplifier and Kozisek discloses a

[27] Arigna's arguments regarding this separate combination are addressed *infra*.

transconductance amplifier, this argument fails. *See* CRB at 73. Dr. Souri testified clearly and specifically regarding the reasons one of ordinary skill in the art would be motivated to make the combination based on the requirements of Soneda's switches. *See supra*. Dr. Sechen agreed that one of ordinary skill in the art would perceive the need for "some form of control" for the switch in Soneda. *See* Tr. (Sechen) at 1274:19-1275:20. Moreover, the evidence shows that both current amplifiers and transconductance amplifiers are addressed together in textbook references. *See* RIB at 20: RX-1629.5; RX-1630.31. And Dr. Sechen admitted that one of ordinary skill in the art would search international patent classification H03F, which includes Kozisek, when looking for circuitry relating to controlling offset cancellation in a current amplifier. *See* Tr. (Sechen) at 1283:17-1284:17; RX-2080[28]; *see generally Wyers v. Master Lock Co*., 616 F.3d 1231, 1237-38 (Fed. Cir. 2010) (discussing standard for analogous art).

Based on the evidence, and in view of the lack of persuasive secondary considerations of non-obviousness, *see infra*, the undersigned finds that Soneda in combination with the control circuitry disclosed in Kozisek renders obvious claims 13 and 29 of the '082 patent.

3. Anticipation by Tedja (Claim 1 and 17)

Tedja is a journal article published by the IEEE in February 1995, which is prior art to the '082 patent. RX-1238. Respondents contend that claims 1 and 17 of the '082 patent are anticipated by Tedja. RIB at 59-72; RRB at 29-31; *see* Tr. (Souri) at 1159:13-1170:25. Arigna argues that Tedja does not anticipate any claim because it fails to disclose the claimed "switching device" and certain related limitations. CIB at 107-110; CRB at 27-60; *see* Tr. (Sechen) at

[28] The Examiner in a continuation application of the '082 patent found that Kozisek rendered obvious certain claims based on this logic. *See* RX-1256.70-72; RIB at 79; *see also* Tr. (Souri) at 1175:25-1176:2.

1250:17-1260:6. Staff agrees with Respondents that Tedja anticipates claims 1 and 17. SIB at 66-72; SRB at 22-23.

b. Claim 1

i. "A circuit comprising"

Dr. Souri identifies a circuit architecture in Tedja that includes a "high output impedance current mode amplifier (IAMP)" and an "offset-current cancellation circuit." Tr. (Souri) at 1159:13-18; RDX-0001C.75; *see* RX-1238 at 3, Fig. 2. Based on this undisputed evidence, the undersigned finds that Tedja discloses a circuit.

ii. "a current amplifier"

Dr. Souri identifies a "high output impedance current mode amplifier (IAMP)" disclosed in Tedja. Tr. (Souri) at 1159:19-1160:2; RDX-0001C.76; *see* RX-1238 at 3, Fig. 2. Dr. Souri explains that the current amplifier in Tedja includes transistors that are paired together as a current mirror and describes a current gain of 10. Tr. (Souri) at 1160:3-1161:4; RDX-0001C.77; *see* RX-1238 at 5 ("The IAMP has a current gain of 10 which is provided by the PMOS current mirror M_3 and M_{outp}."). Based on this undisputed evidence, the undersigned finds that Tedja discloses a current amplifier.

iii. "an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device"

Dr. Souri identifies an "offset-current cancellation circuit" disclosed in Tedja. Tr. (Souri) at 1161:5-20; RDX-0001C.78; *see* RX-1238 at 3 ("The offset-current cancellation circuit is used to remove the remove the offset current coming out of the IAMP"). In reference to Figure 4 of Tedja, Dr. Souri explains that the offset-current cancellation circuit includes a controlled current source comprising transistor M_{outn1}, capacitor C_{adj}, and an operational transconductance amplifier

(OTA), which produces a current that is controlled. Tr. (Souri) at 1161:21-25, 1162:7-17; RDX-0001C.79. He identifies a switching device comprising three transistor switches: M_{sw4}, M_{sw5n}, and M_{sw5p}. Tr. (Souri) at 1162:1-6, 1162:18-1163:2.

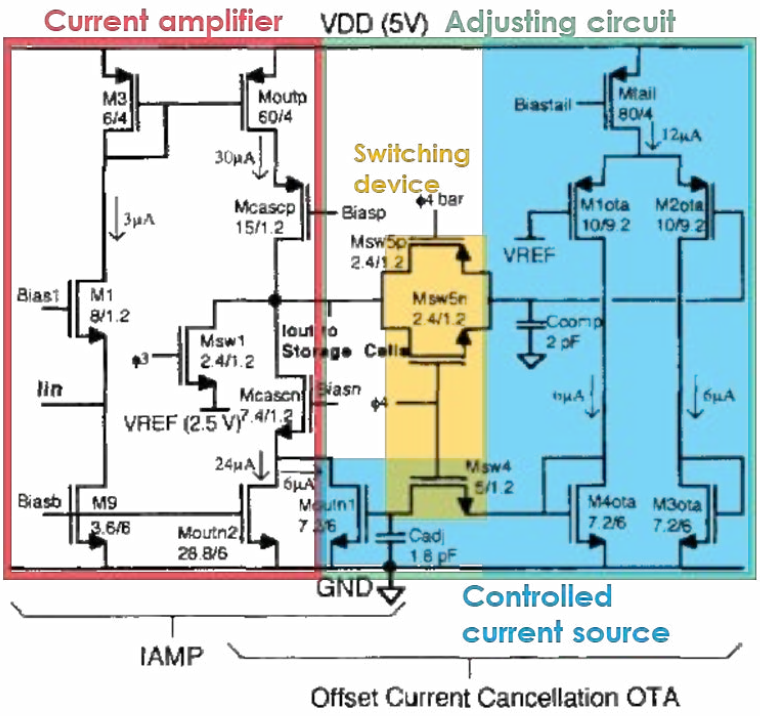

Fig. 4. Schematic of the Current/Charge-Mode Amplifier (IAMP) including the offset-current cancellation circuit.

RDX-0001C.79; *see* RX-1238 at 4 ("Fig. 4 shows the schematic of the current amplifier (IAMP) and the offset-current cancellation circuit."). Dr. Souri explains that the three transistors M_{sw4}, M_{sw5n}, and M_{sw5p} are all controlled by control signal $\phi 4$, and thus turn on and off simultaneously in a coordinated manner. Tr. (Souri) at 1162:18-1163:2.

Arigna argues that the three transistor switches identified by Dr. Souri cannot comprise the claimed "switching device," either "alone or together" (CIB at 108). Specifically, Dr. Sechen submits that the transistor M_{sw4} cannot be the claimed "switching device" because it does not receive the output of the current amplifier. Tr. (Sechen) at 1257:14-20. He submits that

the transistors M_{sw5n} and M_{sw5p} cannot be the claimed "switching device" because they are not connected to the transistor that provides the current value for correcting the offset current. *Id*. at 1257:21-1258:4.

Respondents argue in reply that Dr. Sechen's requirements for the claimed "first switching device" are not recited in the claims of the '082 patent. RRB at 29-30. Staff agrees with Respondents that the claims do not require the connections specified by Arigna. SIB at 68-71.

In consideration of the parties' arguments, the undersigned agrees with Respondents and Staff that the claim language does not require the claimed "first switching device" to be connected to a transistor that provides the current value for correcting the offset current. *See* RRB at 29-30. Arigna's further arguments are addressed in the context of each "wherein" clause below, and show that the "first switching device" requirement of claim 1 is met by Tedja.[29]

iv. "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier"

Dr. Souri identifies 6 microamps of current that are output from controlled current source to the current amplifier indicated on Figure 4 of Tedja. Tr. (Souri) at 1163:3-21; RDX-0001C.80; *see* RX-1238 at 5 ("[T]he output stage of the IAMP becomes the output stage of the offset current cancellation OTA."). Based on this unrebutted evidence, the undersigned finds

[29] Arigna does not appear to contest that three transistor switches operating together can form the claimed "first switching device." *See* CIB at 108 (arguing that the transistors in the asserted "first switching device" are insufficient, "alone or together"). In any case, the record does not indicate that the "first switching device" of the '082 patent cannot read onto multiple transistor switches operating in a coordinated manner. *See, e.g.*, '082 patent at 1:51-53.

that Tedja discloses an adjusting circuit meeting the limitations of the first "wherein" clause of claim 1 of the '082 patent.

v. "wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop"

Dr. Souri submits that there is a connection between the output of the current amplifier and an input of the controlled current source through the three switches he identifies as the "first switching device." Tr. (Souri) at 1163:22-1164:6; RDX-0001C.81; *see* RX-1238 at 5 ("During $\phi 4$, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned on, and the output stage of the IAMP becomes the output stage of the current cancellation OTA."). Dr. Souri identifies a "regulation element of a control loop" that is formed when the switches are closed, which results in a differential current to the OTA that allows the OTA to produce an output current that cancels the offset of the current amplifier. Tr. (Souri) at 1164:18-1165:14; RDX-0001C.82; *see* RX-1238 at 5 ("The gate voltage of M_{outn1} is adjusted so that the IAMP output current offset is zero."). The location of the asserted "input of the controlled current source" and "output of the current amplifier" is shown by the blue node and red node, respectively, in the annotated demonstrative below:

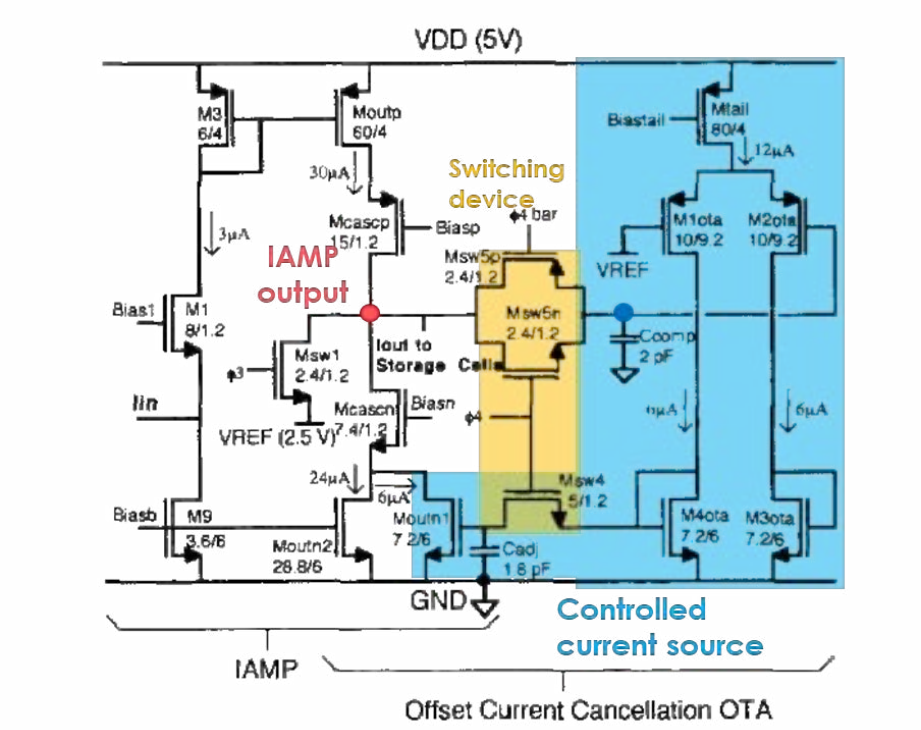

Fig. 4. Schematic of the Current/Charge-Mode Amplifier (IAMP) including the offset-current cancellation circuit.

RDX-0001C.81; RX-1238, Fig. 4 (annotated); Tr. (Souri) at 1166:6-12.

Arigna argues that the "connectable" element of this limitation is not satisfied because the OTA breaks the current path, and this precludes any connection between the output of the current amplifier and the input of the controlled current source. CIB at 110; CRB at 69. Dr. Sechen submits that the input to the controlled current source in Tedja is the gate of transistor M_{outn1}, which does not receive current from the output of the current amplifier through the OTA. Tr. (Sechen) at 1258:7-1259:7. Arigna also argues that the evidence fails to show how a "regulation element of a control loop" exists. CRB at 69.

Respondents argue in reply that the connection between the output of the current amplifier and the OTA meets this limitation, because Dr. Souri has identified the OTA as part of the claimed controlled current source. RRB at 29-31. Dr. Souri explained that "the OTA is part

of that controlled current source" because "it produces a current that is controlled" and outputs a current that is "used to charge the capacitor Cadjust, which then biases the gain of the transistor to Moutn1." Tr. (Souri) at 1162:11-17. Staff agrees with Respondents that the OTA can be part of the claimed "controlled current source, citing disclosures in Tedja that the OTA is part of the "offset-current cancellation circuit." SRB at 22-23; *see* RX-1238 at 4 ("The offset-current cancellation circuit consists of an OTA, three switches: M_{sw4}, M_{sw5n}, and M_{sw5p}, and two capacitors: C_{comp} and C_{adj}."). Staff further argues that the claimed "control loop" only requires a logical signal path, not a current loop. SIB at 69; SRB at 22.

In consideration of the parties' arguments, the undersigned agrees that the evidence shows, clearly and convincingly, that Tedja discloses an "input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop." Dr. Souri's testimony (summarized above) shows clear support that this limitation has been met. *See* Tr. (Souri) at 1163:22-1164:6; RDX-0001C.81; RX-1238 at 5 ("During ϕ4, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned on, and the output stage of the IAMP becomes the output stage of the current cancellation OTA."); Tr. (Souri) at 1164:18-1165:14; RDX-0001C.82. Dr. Sechen's assertion that there is no connection to an "input to the controlled current source," which he identifies as M_{outn1}, fails to address Dr. Souri's argument, which does not identify M_{outn1} as the asserted "input to the controlled current source," but rather the blue node set forth in RDX-0001C.81. *See* Tr. (Souri) at 1166:6-12; RRB at 30. Arigna's argument that the OTA "breaks the current path" between "the output of the current amplifier (red node labelled I_{out}) and the input of the controlled current source (gate of M_{outn1} to the OTA)" (CIB at 110) similarly fails to address Dr. Souri's identification of the "input of the controlled current source."

The undersigned also agrees with Respondents and Staff that the OTA can be part of the claimed "controlled current source." Tedja explicitly identifies the OTA as part of the "offset-current cancellation circuit" and explains that during the offset cancellation phase, "the output stage of the IAMP becomes the output stage for the offset current cancellation OTA." RX-1238 at 4-5; Tr. (Souri) at 1162:7-1163:21; RDX-0001C.79-80. Moreover, as discussed above in the context of Soneda, the claimed "control loop" is only required to be a signal loop, and Dr. Souri explains that a feedback process in Tedja involving the OTA is used to "charge[] Cadjust and bias[] Moutn1 to result in cancellation of the offset current." *See* Tr. (Souri) at 1164:18-1165:14; RDX-0001C.82.

Accordingly, the evidence shows clearly and convincingly that Tedja discloses an adjusting circuit meeting the limitations of the second "wherein" clause of claim 1 of the '082 patent.

vi. "wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element"

Dr. Souri identifies a holding element in Tedja wherein M_{outn1} cancels the offset current using the value stored in capacitor C_{adj}. Tr. (Souri) at 1165:15-1166:2; RDX-0001C.83; *see* RX-1238 at 5 ("The required gate voltage of M_{outn1} to make the offset current zero is stored at capacitor C_{adj}"). He explains that this holding element is formed when the switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned off, disconnecting the input of the controlled current source from the output of the current amplifier. Tr. (Souri) at 1166:3-12; RDX-0001C.83; *see* RX-1238 at 5 ("Once this phase is completed, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned off, the output stage is given up by the OTA to the IAMP, and the IAMP, with its offset current zeroed, is ready to acquire signals from the differentiator.").

Arigna argues that the switches in Tedja cannot disconnect the controlled current source from the current amplifier, because they were not connected by these switches. CIB at 110; CRB at 70. Dr. Sechen submits that the OTA is completely disconnected from the transistor he identifies as the controlled current source during the holding period and so "it would not be appropriate to label the blue node as an input to the controlled current source." Tr. (Sechen) at 1259:15-1260:2.

Staff agrees with Respondents that Tedja meets this limitation. SRB at 22-23.

In consideration of the parties' arguments, the undersigned agrees with Respondents and Staff that this limitation is met by Tedja. Arigna's arguments with respect to the "disconnected" limitation are the same as those addressed above for the "connectable" limitation, and as discussed above, the undersigned does not agree with Dr. Sechen that the OTA cannot be part of the controlled current source. Dr. Souri has identified a holding element that is formed when the switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned off. Tr. (Souri) at 1165:15-1166:12; *see* RX-1238 at 5, Fig. 4. Accordingly, the evidence shows clearly and convincingly that Tedja discloses an adjusting circuit meeting the limitations of the third "wherein" clause of claim 1 of the '082 patent.

vii. "wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current"

As discussed above, Dr. Souri identifies a "regulation element" of a control loop wherein the OTA produces an output current that cancels the offset of the current amplifier. Tr. (Souri) at 1164:18-1165:14, 1166:13-19; RDX-0001C.84; *see* RX-1238 at 5 ("The gate voltage of M_{outn1} is adjusted so that the IAMP output current offset is zero."). Based on this unrebutted evidence, the

undersigned finds that Tedja discloses an adjusting circuit meeting the limitations of the fourth "wherein" clause of claim 1 of the '082 patent.

viii. "wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current"

As discussed above, Dr. Souri identifies a holding element in Tedja wherein M_{outn1} cancels the offset current using the value stored in capacitor C_{adj}. Tr. (Souri) at 1165:15-1166:2, 1166:2-1167:3; RDX-0001C.85; *see* RX-1238 at 5 ("The required gate voltage of M_{outn1} to make the offset current zero is stored at capacitor C_{adj}. Once this phase is completed, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned off, the output stage is given up by the OTA to the IAMP, and the IAMP, with its offset current zeroed, is ready to acquire signals from the differentiator."). Based on this unrebutted evidence, the undersigned finds that Tedja discloses an adjusting circuit meeting the limitations of the final "wherein" clause of claim 1 of the '082 patent.

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Accordingly, the undersigned finds that Tedja anticipates claim 1 of the '082 patent.

b. Claim 17

Respondents contend that Tedja anticipates claim 17 of the '082 patent for many of the same reasons discussed above for claim 1. RIB at 71-72; *see* Tr. (Souri) at 1167:9-1168:17.

i. "A method for correcting an offset of an output current of a current amplifier of a circuit"

As discussed above in the context of claim 1, Tedja discloses a method for correcting an offset of an output current of a current amplifier. *See* Tr. (Souri) at 1167:9-1168:17; RX-1238 at 3 ("The offset-current cancellation circuit is used to remove the remove the offset current coming out of the IAMP"). For the same reasons discussed above in the context of claim 1, the

undersigned finds that Tedja discloses a method meeting the preamble limitations of claim 17 of the ’082 patent.

ii. “connecting a controlled current source to an output of the current amplifier via a first switching device to form a regulation element of a control loop”

As discussed above in the context of the “connectable” limitation of claim 1, Tedja discloses a first switching device that can be closed to connect a controlled current source to an out of the current amplifier, forming a regulation element of a control loop. *See* Tr. (Souri) at 1167:9-1168:17; RX-1238 at 5 (“During ϕ4, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned on, and the output stage of the IAMP becomes the output stage of the current cancellation OTA.”). For the same reasons discussed above in the context of claim 1, the undersigned finds that Tedja discloses a step that meets the “connecting” limitation of claim 17 of the ’082 patent.

iii. “regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element”

As discussed above in the context of claim 1, Tedja discloses a regulation element that regulates an offset current to a minimum. *See* Tr. (Souri) at 1167:9-1168:17; RX-1238 at 5 (“The gate voltage of M_{outn1} is adjusted so that the IAMP output current offset is zero.”). In addition, Dr. Souri explains that the regulation phase occurs when there are gaps between beam crossings that are detected. Tr. (Souri) at 1167:14-1168:5. He explains that during these gaps there is “no input signal or zero input signal, which is a constant value.” *Id*.

Based on this unrebutted evidence, the undersigned finds that Tedja discloses a step that meets the “regulating” limitation of claim 17 of the ’082 patent.

iv. "disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current"

As discussed above in the context of the "disconnected" limitation of claim 1, Tedja discloses a holding element that is formed when a first switching device is open. *See* Tr. (Souri) at 1167:9-1168:17; RX-1238 at 5 ("Once this phase is completed, switches M_{sw4}, M_{sw5n}, and M_{sw5p} are turned off, the output stage is given up by the OTA to the IAMP, and the IAMP, with its offset current zeroed, is ready to acquire signals from the differentiator."). For the same reasons discussed above in the context of claim 1, the undersigned finds that Tedja discloses a step that meets the "disconnecting" limitation of claim 17 of the '082 patent.

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Accordingly, the undersigned finds that Tedja anticipates claim 1 and claim 17 of the '082 patent.

4. Obviousness Based on Tedja, or Tedja in View of Kozisek (Claims 13 and 29)

Respondents contend that claims 13 and 29 are rendered obvious by Tedja alone or Tedja in view of Kozisek. RIB at 73-75. Staff agrees with Respondents that these claims are rendered obvious by Tedja. *See* SIB at 72; SRB at 23-24.

As explained by Dr. Souri, Tedja discloses a $\phi 4$ signal controlling switches M_{sw4}, M_{sw5n}, and M_{sw5p}. Tr. (Souri) at 1168:18-1169:10; RDX-0001C.89. Because the timing of these signals is on the order of microseconds, Dr. Souri submits that one of ordinary skill in the art would understand that electronic control is required. Tr. (Souri) at 1168:18-1169:10; *see* RX-1238 at 5 (describing "the gap between bunches of about 2.5 μs"). Dr. Souri further cites the disclosures in Kozisek describing control circuitry for similar switches. Tr. (Souri) at 1169:14-21. He explains

that one of ordinary skill in the art would have been motivated to use such circuitry with a reasonable expectation of success. *Id*. at 1169:22-1170:21.

As with the combination of Soneda and Kozisek discussed above, Arigna does not specifically dispute Respondents' obviousness arguments based on combining Tedja (for purposes of all claim limitations in claims 1 and 17) with Kozisek (for purposes of the added "control circuit" limitations of claims 13 and 29). *See* CIB at 111-116; CRB at 76-77; SRB at 23-24; discussion *supra*. Arigna also does not provide any substantive dispute regarding the argument that claims 13 and 29 are rendered obvious by Tedja alone.

For these reasons, and in view of the lack of persuasive secondary considerations of non-obviousness), the undersigned thus finds that claims 13 and 29 of the '082 patent are obvious in view of Tedja alone and in view of Tedja in combination with the control circuitry disclosed in Kozisek.

5. Obviousness Based on Kozisek in View of Soneda or Tedja

As discussed *supra*, Kozisek is a U.S. Patent entitled "Amplifier Offset Cancellation Using Current Copier," issued on April 11, 2000, which is prior art to the '082 patent. RX-2080. Respondents contend that Kozisek in view of Soneda or Tedja renders obvious claims 1, 13, 17, and 29 of the '082 patent. RIB at 75-90; Tr. (Souri) at 1171:1-1184:4. In particular, Respondents contend that it would have been obvious to combine the adjusting circuit disclosed in Kozisek with the current amplifier disclosed in Soneda or Tedja to obtain the claimed invention.

Arigna argues that Kozisek does not render obvious any claim because it does not disclose a current amplifier and Respondents have not shown a motivation to combine the circuit in Kozisek with a current amplifier. CIB at 111-14; CRB at 71-74; Tr. (Sechen) at 1261:2-

1263:17. Arigna also argues that Kozisek does not disclose a regulation element of a control loop. CIB at 114-16; CRB at 75-76; Tr. (Sechen) at 1263:18-1265:4. Arigna further argues that because of these failures, no combination of Soneda, Kozisek, or Tedja renders obvious claims 13 and 29. CIB at 116; CRB at 75-77. In addition, Arigna identifies evidence of commercial success for the accused products and the domestic industry products as secondary considerations of non-obviousness. CIB at 116-17; CRB at 77; Tr. (Sechen) at 1266:11-1267:25.

Staff agrees with Arigna that Kozisek does not render any of the asserted claims obvious because it does not disclose a current amplifier, and Staff submits that Respondents have not identified a sufficient reason to combine the circuit in Kozisek with a current amplifier. SIB at 74.

a. Claim 1

i. "A circuit comprising"

Kozisek describes "[a] differential amplifier circuit [that] achieves offset cancellation by supplying an offset correction current from a current copier circuit to the output of the differential amplifier." RX-2080, Abstract; *see* Tr. (Souri) at 1171:1-5; RDX-0001C.93. Based on this undisputed evidence, the undersigned finds that Kozisek discloses a circuit.

ii. "a current amplifier"

Kozisek does not disclose a current amplifier—it describes offset cancellation for an operational transconductance amplifier ("OTA"). *See* RIB at 77-80; CIB at 111-14. Dr. Souri submits that it would have been obvious for one of ordinary skill in the art to replace the OTA in Kozisek with a current amplifier. Tr. (Souri) at 1171:6-1175:1. Dr. Souri explains that the OTA in Kozisek outputs an amplified current from a voltage input and that Kozisek discloses an adjusting circuit for correcting an offset of the amplified current—in his opinion this adjusting

circuit could also correct an offset of an amplified current from a current amplifier. *Id*. at 1172:15-1173:16; RDX-0001C.94-.97. He explains that "a person of ordinary skill would be motivated to . . . expand the application or the utility of Kozisek's adjusting circuit so that it can cancel the offset current of a current amplifier as well." Tr. (Souri) at 1173:17-1174:9. He submits that such a combination would have a reasonable expectation of success because "there would be no modifications necessary to the adjusting circuit of Kozisek." *Id*. at 1174:10-1175:1. Respondents further cite a statement in the prosecution history of a continuation application in the family of the'082 patent, where the examiner found certain pending claims to be obvious in view of Kozisek, reasoning that "[w]hen the current is input, persons skilled in the art can easily think of replacing the operational transconductance amplifier of reference with the current amplifier, which belongs to a common technical measure in this field." RX-1256.70-72.

Arigna argues that Dr. Souri's testimony is conclusory and fails to establish any motivation to replace Kozisek's OTA with a current amplifier. CIB at 111-12. Dr. Sechen testifies that Soneda already discloses an adjusting circuit for its current amplifier and there would be no reason to use Kozisek's adjusting circuit in place of the circuitry disclosed in Soneda. Tr. (Sechen) at 1261:17-1262:11. Dr. Sechen submits that Kozisek's adjusting circuit is substantially the same as the Soneda's adjusting circuit, "[s]o the current amplifier of Soneda plus this adjusting circuit [in Kozisek] equals Soneda." *Id*. at 1261:17-1263:17. With respect to Tedja, Dr. Sechen submits that "because Tedja has two series devices in its output current path," adding Kozisek's adjusting circuit "will cause a total failure." *Id*. at 1261:17-1262:11. Staff agrees with Arigna that Respondents have failed to show why a person of ordinary skill in the art would have looked to Kozisek to correct the offset of a current amplifier. SIB at 73.

In reply, Respondents cite evidence from Dr. Sechen's testimony and other patent proceedings showing that persons of ordinary skill in the art would consider circuitry related to a transconductance amplifier when working on current amplifiers. RRB at 32-33. Respondents argue that there is no evidence of teaching away and that Dr. Sechen's testimony criticizing the combinations of Kozisek with Soneda and Tedja is not reliable. *Id*. at 33-34.[30]

In consideration of the parties' arguments, the undersigned finds that one of ordinary skill in the art would have reason to use the adjusting circuit disclosed in Kozisek with an amplifier such as that in Soneda. The problem of offset currents in current amplifiers was known in the prior art, as specifically recognized in Soneda. *See* RX-2096 at 4 ("In the above-described conventional current-output-type circuit, there are problems in that S/N tends to deteriorate owing to the offset current."). Kozisek clearly discloses an adjusting circuit for correcting an offset current. *See* RX-2080 at Abstract ("The current copier generates an equal and opposite offset cancellation current which is summed with the offset current from the amplifier."); *id.* at 1:5-10 ("The present invention relates generally to differential amplifiers . . . and more particularly, to an apparatus and method for canceling any offsets inherent in such differential amplifier"). The Supreme Court has held that "any need or problem known in the field and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR*, 550 U.S. at 420. Soneda describes a need for circuitry capable of canceling an offset current in a current amplifier, and the undersigned agrees with Dr. Souri that one of ordinary skill in the art would have reason to meet this need through combining the adjusting circuit of

[30] Respondents also argue that Arigna waived certain arguments based on Dr. Sechen's testimony because they were not raised in its Pre-Hearing Brief. RRB at 33. Dr. Sechen's testimony was offered without objection, however, and it is consistent with Arigna's contentions regarding Kozisek. *See* Tr. (Sechen) at 1261:17-1262:11; CPHB at 115-20. Accordingly, the undersigned finds that there has been no waiver.

Kozisek with the amplifier of Soneda. *See* Tr. (Souri) at 1173:17-1174:9 (person of ordinary skill would be motivated to "expand the application or the utility of Kozisek's adjusting circuit so that it can cancel the offset current of a current amplifier as well"); *id.* ("[A] person of ordinary skill would understand that current amplifiers could benefit and improve by the use of the Kozisek adjusting circuit because of its ability to cancel its offset current on the output."); *see Thomson Licensing SAS v. Int'l Trade Comm'n*, 527 Fed. Appx. 884, 889 (Fed. Cir.2013) (finding motivation to combine where references "share common goal"); *KSR*, 550 U.S. at 417 ("if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill").

Both Dr. Souri and Dr. Sechen agree that Kozisek's offset correction circuitry is compatible with the current amplifier disclosed in Soneda. *See* Tr. (Souri) at 1174:10-1175:1 (explaining that there would be a reasonable expectation of success in combining Kozisek's circuitry with Soneda or Tedja); Tr. (Sechen) at 1261:17-1262:5 ("[I]f you were to replace this OTA here with the current amplifier of Soneda, you would get the same thing as Soneda"). Dr. Sechen concedes that Kozisek's adjusting circuit is substantially the same as Soneda's. Tr. (Sechen) at 1262:12-1263:17.[31] The fact that Soneda discloses its own offset correction circuit

[31] Arigna relies on this testimony to argue that Soneda's disclosure of its own adjusting circuit is evidence that one of ordinary skill would not be motivated to modify Soneda to implement Kozisek's adjusting circuit, CIB at 113-14, but this mischaracterizes the obviousness argument. Dr. Souri does not suggest that one of ordinary skill in the art would be motivated to replace Soneda's adjusting circuit—rather, Soneda provides clear evidence that one of ordinary skill in the art would recognize a need for circuitry correcting an offset of a current amplifier and thus provides a reason to combine Kozisek's offset correction circuitry with a current amplifier such as that in Soneda. *See* Tr. (Souri) at 1173:17-1174:9 (discussing motivation to combine). In addition, the adjusting circuit of Soneda and Kozisek are not precisely identical. *See* Tr. (Sechen) at 1261:17-1262:3. Arigna's arguments that one would not, as a general matter, combine a reference relating to transconductance amplifiers with one relating to current amplifiers are rejected for the reasons discussed in Part IV.H.2 *supra*.

that is very similar to Kozisek further demonstrates that one of skill in the art implementing such a circuit would have had a reasonable expectation of success and, indeed, that the results would have been predictable. *See KSR*, 550 U.S. at 417 ("If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability."); *id.* at 416 ("when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result").

The undersigned agrees with Arigna and Staff, however, that the combination of Kozisek's adjusting circuit with Tedja's current amplifier is less convincing. The evidence does not show, clearly and convincingly, that the circuitry in Kozisek could be combined with Tedja with a reasonable expectation of success. *See* Tr. (Sechen) at 1261:17-1262:11 (suggesting that the Kozisek's adjusting circuit would fail if combined with Tedja).[32]

Accordingly, the evidence shows, clearly and convincingly, that one of skill in the art would have reason to use the adjusting circuit in Kozisek to correct the offset current of a current amplifier, as disclosed in Soneda, with a reasonable expectation of success. The undersigned finds that Respondents have failed to carry their burden to as to the combination of Tedja and Kozisek, however.

iii. "an adjusting circuit configured to correct an offset of an output current of the current amplifier, the adjusting circuit having a controlled current source and a first switching device"

Dr. Souri identifies circuitry associated with the "current copier" disclosed in Kozisek that is configured to correct an offset current. Tr. (Souri) at 1176:3-11. Kozisek discloses that

[32] While physical incompatibility does not preclude obviousness, Dr. Souri did not clearly and convincingly show a reasonable expectation of success. Dr. Souri simply testified that "there would be no modifications necessary to the adjusting circuit of Kozisek, so it would have been a matter of routine design and experimentation." Tr. (Souri) at 1174:22-24; *id.* at 1173:10-16.

"[t]he function of this current copier circuit is to 'supply' an offset current having a magnitude that is equal and opposite to the output offset current of OTA 20." RX-2080 at 5:58-61. Dr. Souri identifies a "controlled current source" comprising transistor 62 and storage capacitor 64 and a "first switching device" comprising "third switch 70." Tr. (Souri) at 1176:12-22.

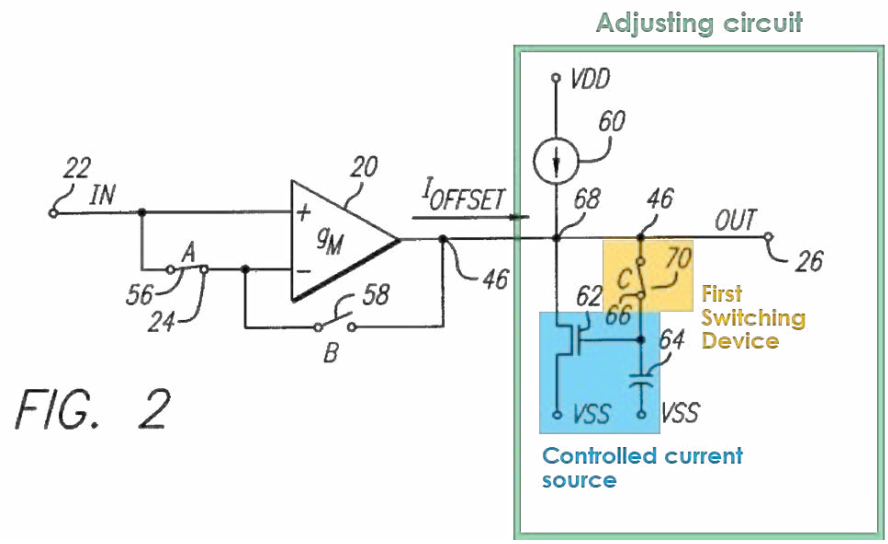

FIG. 2

RDX-0001C.100. RX-2080 at 5:52-54 ("a current copier circuit is conceptually represented by a current source 60, transistor 62, and storage capacitor 64"), 5:63-65 ("a third switch 70 is provided for selectively coupling first terminal 66 of the current copier circuit to output node 46 of OTA 20").

Based on this unrebutted evidence, the undersigned finds that Kozisek in combination with Soneda discloses the components recited in the "adjusting circuit" limitation of claim 1 of the '082 patent.

iv. "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier"

Dr. Souri identifies node 68 of Kozisek as the output of the controlled current source and node 46 as the output of the amplifier. Tr. (Souri) at 1176:23-1177:17; RDX-0001C.101. He

explains that the output current of the controlled current source is produced in the current amplifier in a similar manner to what is disclosed in '082 patent specification. Tr. (Souri) at 1177:18-1178:9; RDX-0001C.102.

Based on this unrebutted evidence, the undersigned finds that Kozisek in combination with Soneda discloses an adjusting circuit meeting the limitations of the first "wherein" clause of claim 1 of the '082 patent.

v. "wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop"

Dr. Souri identifies a regulation element of a control loop that is formed when switch 70 is closed, "allowing for information about the offset current to result in developing a voltage across capacitor 64, which biases transistor 62 to take or subtract the offset current away from the output in a controlled and regulated manner." Tr. (Souri) at 1178:10-1179:10; RDX-0001C.103; *see* RX-2080 at 6:17-22 ("In this phase, also known as the cancellation mode, . . . third switch 70 is closed for allowing the current copier circuit to sense, and null out, any output current offset at output node 46.").

Arigna argues that there is no control loop in Kozisek because current does not flow through the loop identified by Dr. Souri. CIB at 114-15; Tr. (Sechen) at 1263:19-1264:4 ("There is no control loop in Kozisek . . . This is just straight down burying a current through here.").

In consideration of the parties' arguments, the undersigned agrees with Respondents that Kozisek discloses a regulation element of a control loop. As discussed above in the context of Soneda, the claimed "control loop" is only required to be a signal loop, and Kozisek explicitly discloses such a loop in its "cancellation mode." *See* RX-2080 at 6:16-31; Tr. (Souri) at 1178:10-1179:10; RDX-0001.103-104. Accordingly, the evidence shows, clearly and

convincingly, that Kozisek in combination with Soneda discloses an adjusting circuit meeting the limitations of the second "wherein" clause of claim 1 of the '082 patent.

vi. "wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element"

Dr. Souri identifies a holding element in Kozisek that is formed when switch 70 is opened, disconnecting the input of the controlled current source from the output of the amplifier. Tr. (Souri) at 1179:11-21; RDX-0001C.105; *see* RX-2080 at 6:40-42 ("third switch 70 is opened, causing capacitor 64 to maintain the voltage needed to create the offset cancellation current").

Based on this unrebutted evidence, the undersigned finds that Kozisek in combination with Soneda discloses an adjusting circuit meeting the limitations of the third "wherein" clause of claim 1 of the '082 patent.

vii. "wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current"

Dr. Souri identifies disclosures in Kozisek describing the "cancellation mode" wherein the offset current is canceled out "exactly," regulating the offset to a minimum. Tr. (Souri) at 1179:22-1180:8; RDX-0001C.106; *see* RX-2080 at 6:20-22 ("third switch 70 is closed for allowing the current copier circuit to sense, and null out, any output current offset at output node 64"), 6:22-31 ("the net current supplied to second terminal 68 of the current copier circuit (i.e., the net difference between the amount of current sourced by current source 60 and sunk by transistor 62) exactly balances any output offset current provided by output node 46 of OTA 20.").

Based on this unrebutted evidence, the undersigned finds that Kozisek discloses an adjusting circuit meeting the limitations of the fourth "wherein" clause of claim 1 of the '082 patent.

viii. "wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current"

Dr. Souri identifies disclosures in Kozisek describing the voltage maintained on capacitor 64 maintaining a level that allows for cancellation of the offset current. Tr. (Souri) at 1180:9-20; RDX-0001C.107; *see* RX-2080 at 60:49-53 ("the voltage programmed on storage capacitor 64 causes transistor 62 to continue to draw the desired amount of current such that the current copier circuit supplies the desired offset cancellation current to output node 6 of OTA 20 to cancel the output offset current inherent therein").

Based on this unrebutted evidence, the undersigned finds that Kozisek discloses an adjusting circuit meeting the limitations of the final "wherein" clause of claim 1 of the '082 patent.

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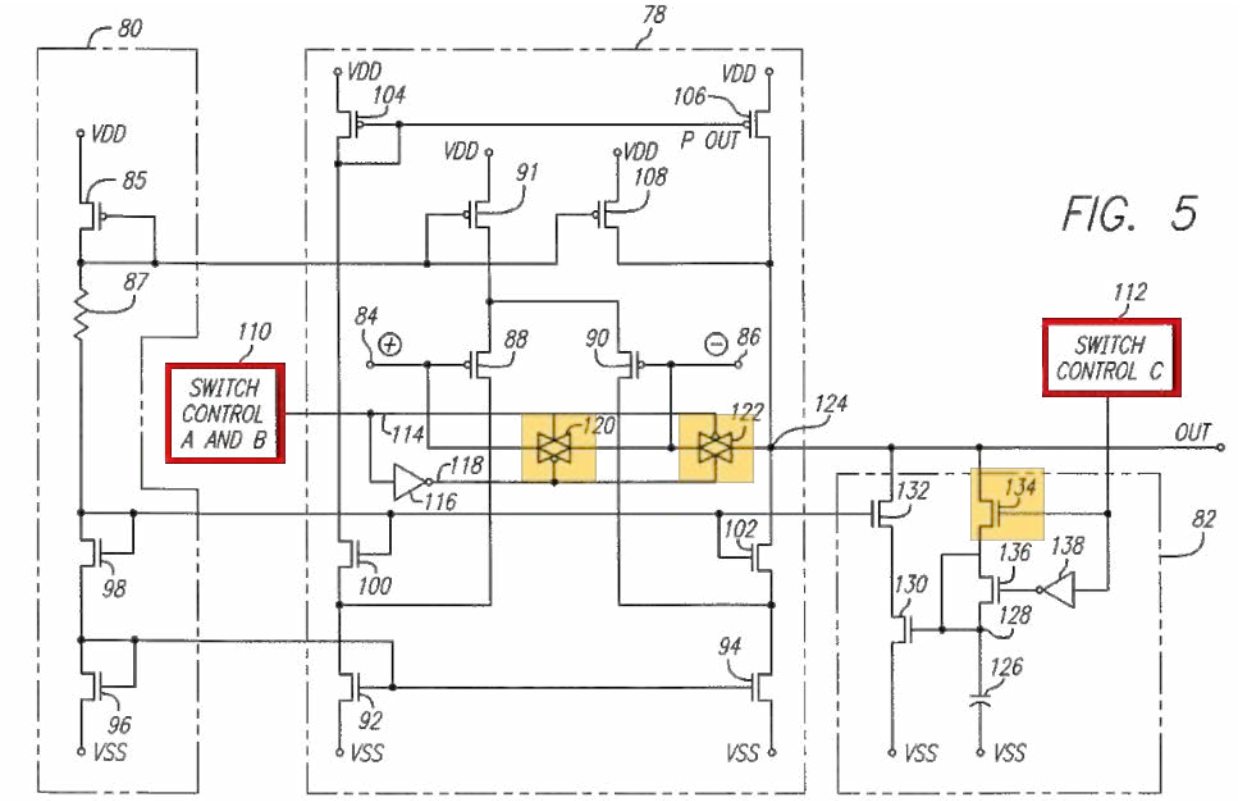
Based on the above, and in view of the lack of persuasive secondary considerations of non-obviousness (*see* Part IV.H.5.e *infra*), the undersigned finds that Kozisek in view of Soneda renders obvious claim 1 of the '082 patent. As discussed above in the context of the "current amplifier" limitation, the undersigned finds that claim 1 has not been shown to be obvious by Kozisek in view of Tedja..

b. Claim 13

Respondents contend that Kozisek in view of Soneda or Tedja renders obvious claim 13. RIB at 88-89. Dr. Souri identifies control blocks disclosed in Kozisek that control the switches

in the adjusting circuit. Tr. (Souri) at 1137:18-1138:4; RDX-0001C.54. Kozisek describes "a control circuit for selecting between a cancellation mode and an operating mode of the differential amplifier." RX-2080 at 3:19-22. With respect to the first switching device, Kozisek identifies "Switch Control C" in block 112, which controls "N-channel transistor 134" corresponding to switch 70. RX-2080 at 8:26-37.



RDX-0001C.113 (citing RX-2080, Fig. 5).

Based on this unrebutted evidence, the undersigned finds that Kozisek discloses a control circuit meeting the limitations recited in claim 13 of the '082 patent. In accordance with the discussion above with respect to claim 1, the undersigned thus finds that Kozisek in view of Soneda renders obvious claim 13 of the '082 patent. For the reasons discussed above in the context of claim 1, the undersigned finds that claim 13 has not been shown to be obvious by Kozisek in view of Tedja.

c. Claim 17

Respondents contend that Kozisek in view of Soneda or Tedja renders obvious claim 17 of the '082 patent for many of the same reasons discussed above for claim 1. RIB at 87-88; *see* Tr. (Souri) at 1181:1-1182:16.

i. "A method for correcting an offset of an output current of a current amplifier of a circuit"

As discussed above in the context of claim 1, Kozisek discloses a method for correcting an offset of an output current, and it would have been obvious for one of skill in the art to use Kozisek's method for a current amplifier, such as the one disclosed in Soneda. *See* Tr. (Souri) at 1171:6-1175:1, 1182:13-16. For the same reasons discussed above in the context of claim 1, the undersigned finds that the preamble limitations are met by the combination of Kozisek and Soneda.

ii. "connecting a controlled current source to an output of the current amplifier via a first switching device to form a regulation element of a control loop"

As discussed above in the context of the "connectable" limitation of claim 1, Kozisek discloses a regulation element of a control loop that is formed when a switch is closed. *See* Tr. (Souri) at 1278:10-1279:10; RX-2080 at 6:17-22 ("In this phase, also known as the cancellation mode, . . . third switch 70 is closed for allowing the current copier circuit to sense, and null out, any output current offset at output node 46."). For the same reasons discussed above in the context of claim 1, the undersigned finds that Kozisek in combination with Soneda discloses a step that meets the "connecting" limitation of claim 17 of the '082 patent.

iii. "regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element"

As discussed above in the context of claim 1, Kozisek discloses a regulation element that regulates an offset current to a minimum. *See* Tr. (Souri) at 1179:22-1180:8; RX-2080 at 6:20-22 ("third switch 70 is closed for allowing the current copier circuit to sense, and null out, any output current offset at output node 64"), 6:22-31 ("the net current supplied to second terminal 68 of the current copier circuit (i.e., the net difference between the amount of current sourced by current source 60 and sunk by transistor 62) exactly balances any output offset current provided by output node 46 of OTA 20."). Dr. Souri identifies disclosures in Kozisek showing that the regulation phase occurs when the differential voltage input is zero. Tr. (Souri) at 1181:1-14; RDX-0001C.110; *see* RX-2080 at 6:17-22 ("In this phase, also known as the cancellation mode, first switch 56 is closed to null the differential input voltage"). Dr. Souri further identifies disclosures in Soneda that describe a zero input current during "regulation . . . to cancel the offset." Tr. (Souri) at 1181:16-1182:12; RDX-0001C.111; RDX-0001C.112.

Arigna argues that this limitation is not met because a POSITA would not be motivated to combine the teachings of Kozisek with the current amplifier of Soneda. *See* CIB at 115-116; CRB at 76.

As discussed above in the context of claim 1, the undersigned finds that one of ordinary skill in the art would have reason to combine the adjusting circuit of Kozisek with a current amplifier as disclosed in Soneda. In this combination, based on the testimony cited above, the evidence shows that one of ordinary skill in the art would have reason to null the current input of Soneda's current amplifier rather than the voltage input of Kozisek's OTA with a reasonable

expectation of success (as shown in Soneda). Accordingly, the undersigned finds that Kozisek in view of Soneda renders obvious the "regulating" limitation of claim 17 of the '082 patent.[33]

iv. "disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current"

As discussed above in the context of the "disconnected" limitation of claim 1, Kozisek discloses a holding element that is formed when a first switching device is open. a holding element in Kozisek that is formed when switch 70 is opened, disconnecting the input of the controlled current source from the output of the amplifier. *See* Tr. (Souri) at 1179:11-21; RX-2080 at 6:40-42 ("third switch 70 is opened, causing capacitor 64 to maintain the voltage needed to create the offset cancellation current"). For the same reasons discussed above in the context of claim 1, the undersigned finds that Kozisek discloses a step that meets the "disconnecting" limitation of claim 17 of the '082 patent except for the "current amplifier" limitation, which is obvious, as discussed above.

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Accordingly, the undersigned finds that Kozisek in view of Soneda renders obvious claim 17 of the '082 patent. For the reasons discussed above in the context of claim 1, the undersigned finds that claim 17 has not been shown to be obvious by Kozisek in view of Tedja.

d. Claim 29

As discussed above in the context of claim 13, Kozisek describes "a control circuit for selecting between a cancellation mode and an operating mode of the differential amplifier." RX-

[33] Arigna's arguments regarding the lack of motivation to combine a reference involving a transconductance amplifier with one involving a current amplifier are rejected for the reasons set forth in Part IV.H.2, *supra*.

2080 at 3:19-22. Because claim 17 is anticipated by Soneda and Tedja, and because claim 17 of the '082 patent is rendered obvious by Kozisek in view of Soneda, the undersigned finds that claim 29 is invalid for the same reasons discussed above in the context of claim 13. For the reasons discussed above in the context of claim 1, the undersigned finds that claim 29 has not been shown to be obvious by Kozisek in view of Tedja.

e. Secondary Considerations of Non-Obviousness

Arigna argues that the commercial success of the accused products and the domestic industry products is evidence for non-obviousness of the claims of the '082 patent. CIB at 116-17; CRB at 77. Respondents argue that Arigna has failed to demonstrate a nexus between the commercial success of any products and the alleged invention of the '082 patent. RIB at 89-90; RRB at 34-35. Staff agrees with Respondents that Arigna has failed to show a nexus between the commercial success of any product and the alleged invention. SIB at 74-75; SRB at 24.

In consideration of the parties' arguments, the undersigned agrees with Respondents and Staff that the record fails to show any commercial success that is relevant to the obviousness of the asserted claims of the '082 patent.

As a threshold matter, the undersigned finds that the record does not show that either the accused products or the domestic industry products have achieved commercial success, which is "usually shown by significant sales in a relevant market." *J.T. Eaton & Co. v. Atl. Paste & Glue Co.*, 106 F.3d 1563, 1571 (Fed. Cir. 1997). The Federal Circuit has held that "[a]n important component of the commercial success inquiry" can be whether the products "had a significant market share." *In re Applied Materials, Inc.*, 692 F.3d 1289 (Fed. Cir. 2012). The record evidence shows that the accused vehicles represent a very small share of the hybrid and electric vehicle market. *See* Tr. (Smith) at 652:19-659:2; CDX-003C.3-11; *see also* Tr. (Graham) at

1002:11-13 ("[T]he accused vehicles are a tiny proportion of all of the electric vehicles."). With respect to the domestic industry products, the record shows that no ATMXT540S chips have [redacted], and the number of ATMXT336S chips [redacted]—both in absolute terms and as a share of Microchip's revenues. *See* Tr. (Reed) at 948:23-949:24; RDX-0002C.5. There is no evidence in the record of Microchip's market share for its [redacted] products, but the ATMXT540S and ATMXT336S only represent [redacted] percent of Microchip's total [redacted] revenue. *See* Tr. (Smith) at 639:10-20. The record does not show that these relatively modest sales and market share represent a level of commercial success for the accused products or the domestic industry products that should be significant to the obviousness inquiry.

The undersigned further agrees with Respondents and Staff that the record does not show a nexus between the purported commercial success of any product and the alleged invention of the '082 patent.[34] With respect to the accused products, Arigna submits evidence that Respondents have touted the importance of the hybrid powertrains of their vehicles. *See* Tr. (Sechen) at 1266:11-1267:25; CDX-007C-19 (citing, *e.g.*, CX-00290; CX-00304; CX-00298). The '082 patent does not claim a hybrid powertrain and it does not claim a power inverter or converter, however—the alleged invention is an adjusting circuit for correcting an offset for a current amplifier. There is no evidence that the Analog Devices chips that are accused of infringing the claims of the '082 patent are an important reason for sales of Respondents'

[34] Arigna is not entitled to a presumption of nexus, because it has not shown that the accused products or the domestic industry products "both embod[y] the claimed features" and are "coextensive with the claims at issue." *SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1319 (Fed. Cir. 2015). Even the chips at issue contain more than the claimed current amplifier circuitry—the Analog Devices products are current sense amplifiers, and the Microchip products are touchscreen controllers. *See* CX-00690 (Analog Devices Datasheet) CX-00057C (Atmel Datasheet).

vehicles.[35] With respect to the domestic industry products, Arigna identifies testimony from Dr. Duvenhage that [redacted] of the domestic industry products. JX-00014C (Duvenhage Tr.) at 21:16-20. But there is no evidence in the record showing that consumers purchase the domestic industry products for their offset correction, rather than features known in the prior art. *See Tokai Corp. v. Easton Enters, Inc.*, 632 F.3d 1358, 1369-70 (Fed. Cir. 2011) ("If commercial success is due to an element in the prior art, no nexus exists.").

Accordingly, the record fails to show evidence of commercial success that would weigh against the obviousness of the '082 patent. The undersigned finds that claims 1, 13, 17, and 29 of the '082 patent are invalid as obvious, for these and the additional reasons discussed above.

V. U.S. PATENT NO. 8,247,867

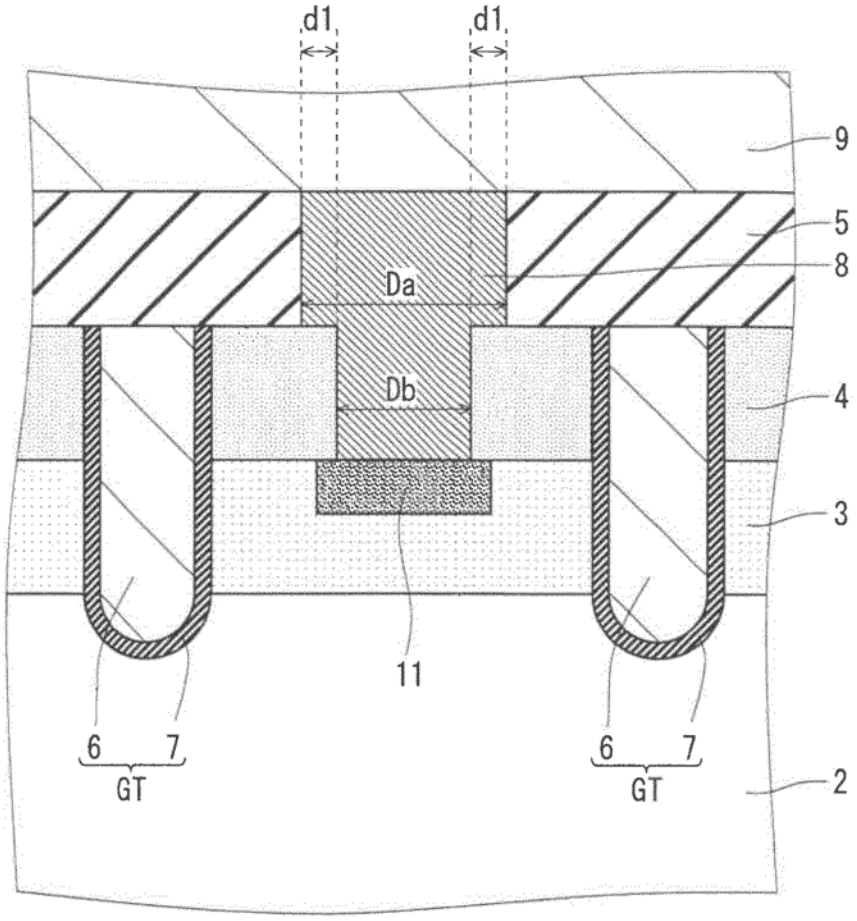
The '867 patent (JX-00004) is titled "Semiconductor Device" and names Kazunari Nakata, Atsushi Narazaki, Shigeto Honda, and Kaoru Motonami as inventors. '867 patent, cover. The patent issued from an application filed on July 15, 2010. *Id*.

A. Specification

The '867 patent describes particular features in a power semiconductor device having a trench gate structure. '867 patent at col. 1:5-8. These semiconductor devices include power metal insulator semiconductor field effect transistors (MISFET) or metal oxide semiconductor field effect transistors (MOSFET). *Id*. at col. 1:9-22. In an embodiment of the invention, a base layer 3 and source layer 4 are formed on an epitaxial layer 2 over a semiconductor substrate 1. *Id*. at col. 3:5-4:15, Fig. 1. Trench gate structures penetrate the source layer 4 and base layer 3.

[35] As discussed *supra*, the Analog Devices chips do not infringe the asserted claims of the '082 patent, which precludes any finding of a nexus.

Id. at col. 4:16-30. An insulating film 5 is formed on the source layer 4. *Id*. at col. 4:31-32. In between the gate structures, a conductive portion 8 penetrates the insulating film 5 and the source layer 4 and connects to a contact region 11 in the base layer 3. *Id*. at col. 4:32-42. In one embodiment, the width of the conductive portion 8 is smaller within the source layer 4 than in the insulating layer 5 (Db < Da). *Id*. at col. 9:66-10:9.



Id. at Fig. 7. A source electrode 9 is formed on the insulating film 5 and connects to the conductive portion 8. *Id*. at col. 4:59-64. Because of the structure of the conductive portion 8, "the stress that is generated in wire bonding for the source electrode 9 is absorbed by the upper surface of the source layer 4 that is in contact with the conductive portion 8." *Id*. at col. 10:41-43.

B. Asserted claims

Arigna asserts claim 4 of the '867 patent for domestic industry and claim 8 for infringement. *See* Order No. 50 at 3 n.4. These claims are reproduced below:

4. A semiconductor device, comprising:

a base layer having a first conductivity type;

a source layer formed on said base layer and having a second conductivity type;

an insulating film formed on said source layer;

a plurality of gate structures penetrating said base layer;

a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer; and

a source electrode formed on said insulating film and electrically connected to said conductive portions, wherein:

said gate structures are formed in a stripe shape in plan view;

parts in which said conductive portions are connected to said base layer are formed, in plan view, side by side in an island shape in a direction of said stripe shape of said gate structures with a distance from said gate structures between said gate structures; and

a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures in a region in which said conductive portions are not connected to said base layer is 0.36 μm or more.

8. A semiconductor device, comprising:

a base layer having a first conductivity type;

a source layer formed on said base layer and having a second conductivity type;

an insulating film formed on said source layer;

a plurality of gate structures penetrating said base layer;

a conductive portion penetrating said insulating film and said source layer, being in contact with an upper surface of said source layer, and electrically connected to said source layer and said base layer; and

a source electrode formed on said insulating film and electrically connected to said conductive portion,

wherein a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10 nm or more and 40 nm or less.

C. Claim Construction

The parties agreed to the construction of several claim terms in the '867 patent. *See* Updated Joint Proposed Claim Construction Chart, EDIS Doc. ID 758271 (Dec. 9, 2021). The terms "are in contact with" and "being in contact with" were agreed to have their plain and ordinary meaning, *i.e.*, "touching." *Id*. at 1. The term "formed on" was agreed to have its plain and ordinary meaning. *Id*. at 2. The term "conductive portion" was agreed to have its plain and ordinary meaning, *e.g.*, "electrically conductive portion." *Id*. The term "upper surface" was agreed to have its plain and ordinary meaning, and the term "source electrode" was agreed to have its plain and ordinary meaning. *Id*.

In the *Markman* order, the term "dimension of a part" in claim 8 was construed to mean "width of a part, measured in a horizontal direction when viewed in cross-section." Order No. 30 at 11-20. In the context of claim 4, the term "dimension of a part" was construed to mean "width of a part, measured in a direction perpendicular to said gate structures in plan view" or the equivalent "width of a part, measured in a horizontal direction when viewed in cross-section." *Id*. at 20-26. The undersigned determined that claim 4 was not indefinite in view of the construction of "dimension of a part." *Id*. at 26-31. The parties agreed that "a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other" has its plain and ordinary meaning. *See* Updated Joint Proposed Claim Construction Chart at 2.

In its post-hearing brief, Arigna addressed the construction of "upper surface," "connected to," and "stripe shape." CIB at 119-125. There is no material dispute regarding the construction of the terms "connected to" and "stripe shape" in claim 4, which should be construed according to their plain and ordinary meaning. *See* RRB at 36; SIB at 81-82; SRB at 26-27. Respondents and Staff note that there are no disputed issues in the investigation that are affected by the construction of these terms. *Id.* With respect to the construction of the term "upper surface" in claim 8, the parties have agreed that this term should have its plain and ordinary meaning, although there is still a dispute regarding the infringement of this limitation. *See* SIB at 79-80; RRB at 36-41. The plain and ordinary meaning of "upper surface" is addressed in the context of infringement, *infra*.

D. Level of Ordinary Skill in the Art

In the *Markman* order, the level of ordinary skill in the art was found to be a bachelor's degree in electrical engineering, physics, materials science, or a similar field, and approximately two years of industry or additional academic experience in semiconductor processing, analysis, design, or development, including a working knowledge of power semiconductor devices. Order No. 30 at 9-10.

E. Importation of Certain Accused Products

As a preliminary matter, the parties dispute whether the accused VW Group vehicles[36] imported into the United States (and thus which are relevant to infringement and violation)

[36] Arigna does not argue that the accused GM vehicles utilize Infineon IGBTs manufactured using [redacted] wafers. *See* CIB at 125-132; RRB at 45 n.8; SRB at 9-10. Arigna also does not dispute that the part numbers for the accused chips used in the accused GM vehicles have part numbers that specify a [redacted]. *See* CIB at 131-132; RIB at 109-110 ("According to Infineon's part numbers for [redacted], the code [redacted]" . . . confirms they are made from [redacted] wafers."); Tr (Bravman) at 744:17-745:11; JX-00020C (Infineon) at 24:4-25:10, 95:10-99:4.

contain only accused Infineon chips that were manufactured using [redacted] wafers, or whether they also include chips manufactured using [redacted] wafers. *See* CIB at 125-132; RIB at 108-111; SIB at 17-19.[37] In this regard, the relevant accused vehicles are the VW ID.4 ([redacted]), Audi [redacted]), and Audi [redacted] containing either: (1) Infineon TRENCHSTOP 5 chip with part number [redacted]; and/or (2) Infineon EDT2 chips with part numbers [redacted]. *See* CIB at 8.

For the reasons below, Arigna has not met its burden to show that accused VW Group vehicles imported into the United States contain accused chips manufactured using [redacted] wafers,

1. The Parties' Arguments

Arigna contends that the accused VW vehicles containing the accused inverters and charge regulators contain Infineon ships made, in at least some instances, from [redacted] wafers. First, Arigna contends that the accused [redacted] inverter contains an Infineon HybridPack Drive power module with part number [redacted], and that "[o]fficial documentation" for this inverter states that the IGBTs contained there are made from [redacted] wafers." CIB at 126-127 (citing CX-01627C). Arigna contends that this evidence outweighs and is not contradicted by testimony from an Infineon witness stating that [redacted] chips made from [redacted] wafers were [redacted] and that, in any case, such chips produced from [redacted] wafers could have been [redacted] and incorporated into the accused vehicles. *See* CIB at 127-128. Second, Arigna argues that an Infineon presentation [redacted] discusses a [redacted]

[37] A "wafer" is a disk-shaped material from which the accused chips are made. *See* Tr. (Arigna Op.) at 29:18-20. The parties also dispute whether chips manufactured using [redacted] wafers are representative of chips manufactured using [redacted] wafers for purpose of the infringement analysis. *See* Part V.F.2 *infra*.

strategy for [redacted] and this presentation indicates that IGBT chips [redacted]" are made from [redacted] wafers because [redacted] using [redacted] wafers. *Id.* at 129-130 (citing RX-2823C at 16, 21, RX-2824C.35, RX2827.47, RX2828C.27). Third, Arigna argues that the accused VW ID.4, Audi [redacted], and Audi [redacted] products all contain a [redacted], and that an Infineon declaration indicates that [redacted]. *Id.* at 130-131 (citing RX-0713C ¶¶ 21-22, RX-2824C, RX2827; JX-00020C ([redacted]) at 58:5-11). Finally, Arigna argues that there is no documentary evidence stating that the accused semiconductor devices were made from [redacted] wafers. *Id.* at 131-132.

Respondents argue, in opposition, that Arigna's arguments regarding importation of [redacted] wafer products are waived. Respondents state that "[t]he only position Arigna ever offered before trial about Infineon's [redacted] wafer products is that they are allegedly representative of Infineon's [redacted] wafer products." RRB at 41-42. Respondents argue that the documents relied upon by Arigna were not discussed before trial, either in depositions or in expert reports, and that previous rulings on Respondents' Motion *in Limine* No. 3 and Respondents' objection to certain cross-examination questions at trial do not permit "the brand-new argument that 'Volkswagen uses [redacted] wafer products.'" *See id.* at 42. Respondents argue that Arigna had notice of Respondents' contention that there was no importation of [redacted] wafer products and that Arigna "never presented any contention, expert opinion, documents, or argument that any Respondent has ever imported Infineon [redacted] wafer products – not until opening arguments at trial." *Id.* at 44.

On the merits, Respondents contend that Arigna has failed to meet its burden of showing that any accused chips in the accused products were made from [redacted] chips. See RIB at 108-111; RRB at 44-52. Respondents argue that the five chips at issue are part of broad Infineon product lines for EDT2 devices and TRENCHSTOP 5 devices "that include many other IGBTs not found in any accused vehicles." RIB at 108. Respondents argue that it is undisputed that Infineon has manufactured chips in the EDT2 and TRENCHSTOP 5 product lines from [redacted] wafers, but that Infineon has moved away from [redacted] wafers and towards manufacture on [redacted] wafers, and that Infineon began [redacted] IGBT production in [redacted]. RIB at 108-109 (citing Tr. (Bravman) at 746:6-25, RX-2828C.16, RX-2824C.34-35, and RX-2827C.50). Respondents contend that the unrebutted evidence, including from the deposition of Infineon witness Mr. [redacted], indicates that the [redacted] chip has never been fabricated on [redacted] wafers and that Infineon had transitioned to making the [redacted] chip and [redacted] chips exclusively on [redacted] wafers "well before the importation or sale of the accused vehicles began." *Id.* at 110.

Respondents further state that Arigna relies upon evidence "upon which there is no deposition or trial testimony" (RRB at 45). With respect to CX-01627C, Respondents argue that "there is no testimony about this spreadsheet, its origins, its creation date, what it applies to, or anything else," and argues that the title of the spreadsheet refers to a [redacted] date. *Id.* at 46. Respondents state that a related document (CX-0136C) dated [redacted] contains the same basic technical information as CX-01627C and that Volkswagen's witness explained that [redacted]

[redacted]. *Id.* at 47.[38] Respondents also argue that Arigna mischaracterizes the testimony of the Infineon witness, that Arigna seeks to invert the burden of proof, and that Arigna's attempts to discredit the testimony of the Infineon witness lack merit. *Id.* at 47-49. With respect to Arigna's arguments regarding manufacture at the [redacted] facility, Respondents state that the cited evidence does not show that this facility makes EDT2 wafers at all, let alone the specific EDT2 products accused in this investigation. *Id.* at 50-51. Respondents argue that Arigna's arguments regarding the [redacted] TRENCHSTOP 5 chip mischaracterizes the Infineon declaration. *Id.* at 51-52. Respondents further argue that "[t]he record makes clear that distinct [redacted] and [redacted] wafer products exist, regardless of whether the part number captures that distinction, and Arigna has not provided evidence that an [redacted] wafer product has been imported." *Id.* at 52.

Staff agrees with Respondents that there is no evidence that the accused imported chips are made from [redacted] wafers. *See* SIB at 17-19. Staff argues that there is no evidence that the "accused model year [redacted] or model year [redacted] VW and Audi vehicles with [redacted] chips or [redacted] chips contain an Infineon chip made on or before [redacted]." *Id.* at 18.[39] Staff contends that Arigna's arguments relying on the CX-1627C spreadsheet and the RX-2823C presentation should be rejected for failure to raise them in the prehearing

[38] Arigna cites CX-00136C in its reply brief to argue that [redacted]." CRB at 91-94 and n. 14. Arigna argues that VW should not be permitted to change its position "from its corporate representative's [redacted] at the end of discovery" to its current argument. *See* CRB at 94-95 (discussing Mr. [redacted] Dec. 9, 2021 deposition testimony).

[39] Staff states that a sales spreadsheet of VW ID.4 sales in the U.S. "appears to show that sales of that vehicle did not begin until [redacted]." SIB at 18 (citing CX-00031C).

brief.[40] On the merits, Staff argues that these arguments do not show use or importation of [redacted] wafers for the accused products. With respect to CX-01627C, Staff states that the title of the spreadsheet indicates a [redacted] date and thus is irrelevant to showing "whether [redacted] chips or [redacted] chips are in the accused vehicles as of [redacted]." SRB at 4. Staff contends that any metadata relating to a more recent date "is far too thin a reed to hang the Complainant's entire importation theory on," and states that Complainant's Post-Hearing Brief fails to identify any foundation for the document, does not identify any Infineon chip by model number, and does not explain who authored the document. *Id.* at 4-5. With respect to RX-2823C, Staff argues that the presentation does not refer to any of the specific chips at issue and that the document indicates [redacted]." *Id.* at 5. Staff contends that Arigna's arguments about discrepancies in the Infineon witness's testimony are incorrect and, even if correct, do not establish that Arigna has met its burden of proof on importation. *Id.* at 6-9. Staff further argues that Arigna's statements about the possibility that [redacted] chips made before [redacted] might have been installed and imported in model year [redacted] vehicles are "mere speculation unbacked by evidence." *Id.* at 9.

Regarding waiver, Arigna states in its reply brief that it has consistently accused "all" [redacted] chips of infringement,[41] and has

[40] Staff argues that "the spreadsheet on which the Complainant places such heavy emphasis (CX-01627C) is identified only in two footnotes in the Complainant's Pre-Hearing Brief, as part of long string cites" and that RX-2823C "does not appear to be cited at all in the Complainant's Pre-Hearing Brief." SRB at 3-4.

[41] Arigna further states that Volkswagen admitted in sworn interrogatory responses that [redacted]. *Id.* at 91.

never claimed it was not accusing [redacted] wafer products of infringement. CRB at 90. Arigna states that its infringement contentions all cited and analyzed infringement by [redacted] wafer products, and that its prehearing brief cited evidence indicating that Volkswagen's accused components and vehicles are imported with [redacted] wafer products. *Id.* at 91 (citing Compl. Pre-Hearing Br. at 10-11 and n.15 and CX-01627C). Arigna states that the argument that Arigna abandoned arguments relating to [redacted] wafer products is incorrect and contradicts rulings regarding one of Respondents' motions *in limine* as well as one of Respondents' objections at the the hearing. *See id.* at 90.

Arigna further argues in reply that Volkswagen's arguments do not cite testimony or documents from Volkwagen, [redacted], or Volkswagen's other component vendors, instead relying on information from Infineon, who Arigna states "like Volkswagen is attempting to invalidate the '867 patent." CRB at 95-96. Arigna states that documents cited by Respondents (in particular, RX-2828C.16 and RX2727C.50) are not "specific to the accused chips, components or vehicles." *Id.* at 96-97. Arigna argues that the Infineon deposition testimony "directly contradicts" Infineon's earlier sworn declaration and that "none of this testimony is specific to any Volkswagen component or vehicle; none of it contradicts either the [redacted] documents produced before it, or the Volkswagen 30(b)(6) testimony provided after it; and none of says that [redacted] wafer products are not imported in the accused components or vehicles." *Id.* at 97. Arigna also argues that it is immaterial that Arigna's technical expert did not opine further on this issue because he is "not an expert in, for example, the semiconductor or automotive supply chain, and he has no personal knowledge of which sized wafers were used to make the accused chips in the accused vehicles and components." *Id.* at 98. Arigna states that

Dr. Bravman admitted as such and thus his "reading certain documents and testimony into the record lends no additional probative weight to Volkswagen's position." *Id.*

2. Discussion

Upon review of the parties' submissions and cited evidence, the undersigned finds that Arigna has not shown, by a preponderance of the evidence, that the accused VW vehicles include accused chips [redacted] made from [redacted] wafers.[42]

a. Waiver and Preclusion Issues

As a preliminary matter, Arigna did not waive the general argument that accused [redacted] chips made from [redacted] wafers have been imported in the accused VW vehicles. VW admitted importation of chips with these part numbers, which part numbers do not indicate whether they are made from [redacted] wafers or [redacted] wafers, and Respondents do not contend that chips with part numbers [redacted] have never been made using [redacted] wafers— only that such chips were phased out before any incorporation into the accused vehicles. *See* RIB at 110 ("[W[ell before the importation or sale of the accused vehicles began, Infineon already had transitioned to using [redacted] wafers exclusively for the [redacted] and [redacted]."); CX-02370C, at 5-9 (VW interrogatory responses identifying [redacted] chips in accused imported products). Further, Respondents and Staff do not dispute that Arigna provided infringement contentions assessing Infineon TRENCHSTOP 5 and EDT2 chips from both [redacted] and [redacted]

[42] As discussed above, Arigna does not dispute that the accused GM vehicles and Infineon EDT2 chips contained therein are made exclusively from [redacted] wafers.

wafers.[43] And despite Respondents' assertion that Arigna never mentioned this argument until the trial (*see* RRB at 44), Arigna's response to Respondents' MIL 3 specifically stated that Arigna contested whether [redacted] wafer products were at issue. *See* Arigna Resp. to Resp. Mot. *in Limine* No. 3, at 1 and n.1 ("Arigna does not agree that only [redacted] wafer products are at issue.") (citing [redacted] Decl.) (EDIS Doc. ID 766636). Under these circumstances, the undersigned does not find that Arigna waived the general argument that the three accused chips at issue encompass [redacted] wafer products.[44]

This does not mean, however, that Arigna was free to introduce wholly new contentions in support of this argument that were not present in its Prehearing Brief, particularly given that Arigna carries the burden of proof. With respect to this issue, the undersigned finds that Arigna's contentions based on CX-1627C are not waived. This document was cited twice in Arigna's prehearing brief as showing use of the [redacted] chip, and Arigna's argument consists of little more than pointing to a line item stating "[redacted] wafer." *See* Compl. Pre-Hearing Br. at 11 n.15 and 146 n.43; CIB at 126-127.

Arigna did, however, waive its affirmative contentions based on Infineon's "[redacted]" strategy. In particular, Arigna's extended discussion at pp. 129-130 of its Initial Post-Hearing Brief that Infineon facilities at [redacted] manufacture only [redacted] wafer products, and Arigna's inferences regarding what this means for the chips at issue, do not appear in Arigna's

[43] Indeed, Respondents moved to exclude expert evidence regarding IGBT's made from [redacted] wafers on the basis that it was irrelevant to the investigation. *See* Respondents' Motion *in Limine* No. 3, at 1-2. That motion was denied. *See* Order No. 45 (Mar. 31, 2022).

[44] Respondents argue that Arigna's previous arguments regarding [redacted] wafers were limited to "representativeness" and not to actual importation, citing Complainants' prehearing brief. *See* RRB at 108. While Complainants' contentions in the prehearing brief appear to focus on representativeness, Complainants clearly accuse the three part numbers at issue (*see* CIB at 8), and the part numbers do not distinguish between [redacted] and [redacted] wafer products.

Prehearing Brief. To the extent Arigna sought to affirmatively rely on these contentions (apart from any testimony elicited from Dr. Bravman at trial), Arigna should have described them at least by its Prehearing Brief. *See* Ground Rule 9.2. Accordingly, Arigna is precluded from establishing that importation has been shown based on Arigna's arguments regarding the [redacted] facility.[45] [46]

b. Importation Evidence

In any case, regardless of waiver issues, Arigna has not met its burden to show that any of the three accused chips at issue, as imported in the accused vehicles, have been made using [redacted] wafers.

(i). [redacted] chip ([redacted])

With respect to the [redacted] chip (a TRENCHSTOP 5 chip, *see* CIB at 8), the evidence fails to show, by a preponderance, importation of accused products using an [redacted] chip from an [redacted] wafer. Infineon's witness, Mr. [redacted] specifically testified that this chip has only been manufactured using a [redacted] wafer, based on his consultation "with the responsible marketing person," and that "[n]o commercial versions of this product have ever been made using an [redacted] wafer." JX-00020C ([redacted] at 18:3-5, 92:7-

[45] While Arigna was permitted to cross-examine Dr. Bravman on this topic (who testified on direct regarding the Infineon facilities), Arigna's extended affirmative argument in its post-hearing briefs does not rely on the testimony of Dr. Bravman. *See* Tr. (Bravman) at 746:15-25; RDX-0003C.41; CIB at 129-131.

[46] Arigna is also precluded from relying upon the "[a]dditional documentary evidence and testimony" cited for the first time in its Reply Post-Hearing Brief, in particular, CX-00136C and the [redacted] deposition. *See* CRB at 91-94. These contentions should have been made, at the least, in Arigna's Prehearing Brief and Initial Post-Hearing Brief. *See* Ground Rule 9.2 and 13.1-13.2. Moreover, Arigna's preclusion argument as to Mr. [redacted] testimony, even if not waived, is rejected. *See* CRB at 94-95. Arigna has not shown that Mr. [redacted] (a VW representative) was required to testify about technical information within the possession, custody, and control of Infineon, including Infineon CBI information. *See* JX-00020C ([redacted] (deposition transcript of Infineon representative marked as CBI).

93:2 ("[t]his component has only been manufactured on [redacted] wafer.").

Arigna argues that this testimony should be disregarded because it purportedly contradicts statements in an earlier declaration provided by Mr. [redacted] as well as certain other deposition testimony from Mr. [redacted] *See* CIB at 131; CRB at 96-97. However, the relevant statements in Mr. [redacted] declaration (RX-713C, ¶¶ 21-22) refer generally to TRENCHSTOP 5 products but do not address any particular chip within that category. Thus, while Mr. [redacted] declaration states that [redacted], it provides no information about the wafers used for specific chip products. *See* RX-713C.[47] Similarly, Mr. [redacted] deposition testimony relating to the [redacted] addresses TRENCHSTOP 5 products generally, and not the status of any particular chip.[48] Thus, the record does not show that Mr. [redacted] deposition testimony regarding the [redacted] chip conflicts with other evidence he provided. *See* RRB at 49-52; SRB at 7-9.

Arigna has also argued that Mr. [redacted] testimony is not credible because of Infineon's interests in "helping its litigation common interest and strategic business partner, Volkswagen, to avoid an exclusion order" and because Mr. [redacted] lacked personal knowledge and relied upon communications from others. CIB at 128; *see also* CRB at 98. However, Arigna has provided no specific reason persuasively indicating that Mr. [redacted] deposition testimony,

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[47] Similarly, Mr. [redacted] declaration states that [redacted] even though it is undisputed that certain Infineon EDT2 products ([redacted]) have only been produced on [redacted] wafers. *See* RX-713C ¶ 4; CIB at 8 (categorizing the "[redacted]" chips as "Infineon EDT2" chips). The evidence also indicates that there are multiple TRENCHSTOP 5 chips. *See* RX-713C ([redacted] Decl.) ¶ 20 ("[redacted]").

[48] Arigna itself acknowledges that chip-specific evidence is important. *See* CRB at 97 (criticizing Respondents based on lack of "chip-specific evidence").

made under penalty of perjury, should not be given any weight or why it was unreasonable of him to prepare for his deposition by consulting with knowledgeable personnel at Infineon. *See* RRB at 49-20; SRB at 6-7. Moreover, Arigna has not provide any affirmative evidence indicating that the [redacted] chip used in the accused vehicles has been produced using [redacted] wafers. Arigna bears the burden of proof on importation and infringement yet has produced no evidence from Infineon or any other knowledgeable entity indicating an [redacted] wafer [redacted] for the accused [redacted] chip.[49] Further, as discussed in Part V.F.2 *infra*, Arigna has not shown that [redacted] wafer products are representative of [redacted] wafer products.

Accordingly, Arigna has not shown by a preponderance of the evidence that the accused [redacted] chips imported in the accused vehicles have been made using [redacted] wafers.

(ii). [redacted] **and** [redacted]

The evidence also does not show by a preponderance that the accused vehicles include [redacted] chips made from [redacted] wafers.

First, the "official documentation" relied upon by Arigna (CX-01627C) is a spreadsheet unaccompanied by any witness testimony identifying it as "official documentation" of these chips or even discussing it. *See* CIB at 126-127. It is unclear what date(s) the document pertains to,[50] or whether it reflects any final version of a product. Moreover, Arigna has not pointed to

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[49] Arigna's arguments based on CX-01627C and RX-2823C relate to the Infineon EDT2 products, and thus (to the extent not waived) are not relevant to analysis of the [redacted] chip (a TRENCHSTOP 5 product). *See* CIB at 126 (citing CX-01627C in support of contentions regarding the [redacted] chip); CIB at 129-130 (discussing RX-2823 and other documents in relation to "EDT2 chips").

[50] As noted by Respondents and the Staff, the title of the document appears to incorporate a [redacted] date, which was before Infineon began moving towards use of [redacted] wafers, and before the date when Mr. [redacted] testified that the chips at issue were made and sold using only [redacted] wafers. *See* CIB at 127; RRB at 46-47; SRB at 4; JX-00020C ([redacted] Tr.) at 55:21-56:8, 57:6-58:18; discussion *infra*. Arigna

any chip-specific information on the spreadsheet indicating that it relates to the products at issue. *See* SRB at 4-5 and n.3; RRB at 46-47. Accordingly, this spreadsheet does not provide reliable and probative evidence that either the [redacted] or the [redacted] chips in the accused vehicles were made using [redacted] chips.[51]

Second, even if the argument were not waived, Arigna's evidence regarding the [redacted] program and capacities of the [redacted] also does not carry its burden of proof. *See* CIB at 129-130; RX-2823C. There is no explanatory witness testimony regarding the primary document relied upon by Arigna (RX-2823C) and the document appears only to provide high-level information regarding [redacted] products generally. *See* CIB at 130; CX-2823C; RRB at 50-51; SRB at 5. In the absence of witness testimony explaining the document, or clear evidence regarding Infineon's [redacted] approach or evidence regarding the scope of Infineon's [redacted] products, the cited evidence and attorney argument also does not carry significant probative value, let alone evidence sufficient to meet Arigna's burden of proof.

Instead, the only clear testimony in the record is that of Mr. [redacted] who testified that [redacted]. *See* JX-00020 ([redacted] Dep.) at 58:20-59:14; *id.* at 87:2-13 and 88:16-89:12[52]; *see also* RX-713C ([redacted] ¶ 6. While it is possible

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states that this document was "last modified" in [redacted] (CIB at 126); however, there is no evidence regarding the scope or content of this modification.

[51] Respondents state that certain deposition testimony relating to an [redacted] document contains "the same basic technical information." RRB at 47. Given the date of the document, and that it appears to relate to [redacted] (*see* CX-00136C, at VW-ITC 00008525), this document similarly does not provide reliable and probative evidence regarding the accused chips as used in the [redacted] accused vehicles. *See* RRB at 47; JX-00019C (Volkwagen) at 33:10-35:19.

[52] Arigna notes that Mr. [redacted] testimony specifically addresses part number [redacted], not [redacted]. *See* CIB at 127-128. However, Mr. [redacted] appeared to identify this chip with and

that certain pre- products were used in accused imported vehicle (which only encompass model years , *see* CIB at 8), Arigna has provided only speculative assertions to support this contention and no evidence regarding supply chains or any other probative evidence in this regard. *Cf.* CRB at 98 (criticizing Dr. Bravman's testimony because he lacked knowledge of the "automotive supply chain"); *see* SIB at 17-19. Further, for the reasons discussed above regarding the chip, Arigna has not shown that Mr. testimony is unreliable or internally inconsistent.

Based on the considerations above, and given that Arigna bears the burden of proof, the record fails to show, by a preponderance, that the chips, as used in the accused products, have been made using wafers.[53]

F. Infringement

Arigna asserts that the accused products infringe claim 8 of the '867 patent. *See* CIB at 134. The infringement disputes and analysis focus on the five Infineon chips contained in the accused vehicles. As discussed *supra*, one of these accused chips is an Infineon TRENCHSTOP 5 chip with part number . The other accused chips are Infineon EDT2 chips with part numbers . *See* CIB at 8; Part V.E *supra*.

Arigna has not shown by a preponderance of the evidence that the imported accused chips infringe claim 8. First, the evidence shows that only products made using chips

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without the . *See* JX-00019C (at 30:1-11; SRB at 6. In addition, Mr. elsewhere stated that , thus encompassing . *See* JX-00019C at 58:20-59:14.

[53] Further, as discussed in Part V.F.2 *infra*, Arigna has not shown that products are "representative" of products.

are relevant to the infringement analysis because Arigna has not shown that any accused chips made using [redacted] wafers have been used in the accused vehicles and also has not shown that accused chips made using [redacted] wafers are representative of chips made using [redacted] wafers. *See* Part V.E *supra* and Part V.F.2 *infra*. Second, an element-by-element analysis of the accused chips made using [redacted] wafers fails to show, by a preponderance, that all elements of claim 8 are satisfied.

1. Background: Evidence Relating to Structures in the Accused Chips

In addressing issues of infringement. the parties rely and/or address certain images of Infineon TRENCHSTOP 5 and EDT2 chips: these are the "Tyndall" images, the "Chipworks" images, and the images produced by Infineon. *See* Tr. (Sechen) at 316:17-317:11; RIB at 100-107.

The Tyndall images were made using scanning electron microscopy ("SEM") and were obtained from a company that performs "imaging of semiconductor devices." Tr. (Sechen) at 317:5-11. The Tyndall image primarily relied upon by Dr. Sechen for the disputed claim limitations (CX-00178C) is of an EDT2 device formed from a [redacted] wafer. *See* Tr. (Sechen) at 358:20-22, 473:12-14; CDX-001C-182, 195.

The Chipworks images (CX-01031C, CX-00688, CX-00689) are also SEM images obtained from a third-party "teardown house." *See* CDX-001C-144 (identifying Chipworks evidence); Tr. (Bravman) at 753:23-754:6. These images were provided in connection with a 2014 report analyzing an Infineon TRENCHSTOP 5 device. *See* RIB at 106; CX-01031C. The Chipworks image primarily relied upon by Dr. Sechen for the disputed limitations (CX-0689C) is of a TRENCHSTOP 5 device formed on an [redacted] wafer. *See* Tr. (Sechen) at 349:9-15; CDX-001C-189 (citing CX-00689C); Tr. (Bravman) at 753:23-754:6; CIB at 147, 158.

The Infineon images were produced by Infineon, the manufacturer of the devices, during the course of the investigation. *See* Tr. (Sechen) at 465:18-466:3. These images were created using transmission electron microscopy ("TEM"). *See* Tr. (Sechen) at 465:18-24; RIB at 100. Infineon produced four sets of images that it stated were representative of the following automotive qualified categories of chips: TRENCHSTOP 5 chips made using [redacted] wafers (CX-0144C); TRENCHSTOP 5 chips made using [redacted] wafers (CX-0143C); EDT2 chips made using [redacted] wafers (CX-0142C); and EDT2 chips made using [redacted] wafers (CX-0141C). *See* RIB at 100; JX-00020C ([redacted] Dep.); RX-713C ([redacted] Decl.) ¶¶ 3, 11, 16, 20, 23, 27. The images were created by individuals at Infineon that Mr. [redacted] stated "[redacted]" RX-713C ([redacted] Decl.) ¶¶ 3, 11, 16, 20, 23, 27.

2. Representativeness of Products Manufactured Using [redacted] Wafers

The parties dispute whether products manufactured using [redacted] wafers are "representative" of products using [redacted] wafers such that evidence for infringement by [redacted] wafer products is sufficient to show infringement by [redacted] wafer products. *Cf. Certain Mechanical Planarization Slurries and Components Thereof*, Inv. No. 337-TA-1204, Comm'n Op., at 9-11; SRB at 2-3 ("to rely on evidence about [redacted] chips, the Complainant is obligated to show either that the accused products that were imported contain [redacted] chips or that [redacted] chips are representative of [redacted] chips").[54]

[54] In particular, Respondents and Staff contend that the [redacted] and [redacted] products have significant structural differences around the interface between the trench contact and source layer. *See* RIB at 112; SIB at 52.

Arigna claims that [redacted] wafer products are "representative" of [redacted] wafer products because certain Infineon [redacted] wafer product images are similar to a Tyndall [redacted] wafer product image (CX-00178C). *See* CIB at 133; CRB at 100-101. In particular, as relevant for infringement purposes, Arigna states that "both the Tyndall image of a [redacted] wafer and the Infineon image of an [redacted] wafer have a pronounced stair-step along the upper surface of the source region" and "similarly sized dimensions of that part." CIB at 133. Arigna claims that any distinctions between the Infineon [redacted] wafer images and the Infineon [redacted] images should be discounted because Arigna's expert testified that these distinctions "were not readily explainable" given the use of the [redacted] for the [redacted] and [redacted] products and because of Infineon's "[redacted]." CIB at 133-134; CRB at 101. Arigna argues that a "designer would not want the [redacted] to be outputting devices with [redacted] 10-20% difference allowed for tolerances" and that the products are "[redacted]." CRB at 99-101. Arigna further states that, according to Infineon's witness, the processes for the [redacted] wafer products and [redacted] wafer products have "[redacted]." CRB at 102.

Respondents argue that Arigna "improperly relies on [redacted] to assert representativeness." RIB at 115. Respondents argue that Arigna's expert, Dr. Sechen, did not address differences in equipment or process recipes. *See id.* Respondents also argue that Arigna's comparison between the Infineon [redacted] image and Tyndall [redacted] image relies upon a "deceptively cropped version of a Tyndall SEM image," and that the Tyndall SEM image relied upon by Arigna shows "curtaining damage" which affected the appearance of the image. *See* RIB at 116-117; RRB at 55-56. Respondents argue that testimony from their expert, Dr. Bravman, is "credible, well supported, and unimpeached" and confirms the distinctions between

[redacted] and [redacted] products "readily apparent in Infineon's TEM images of IGBTs from [redacted] and [redacted] wafers." RIB at 117-118. Respondents further argue that there are more [redacted] in the [redacted] and [redacted] mask sets that Dr. Sechen did not review. *See* RRB at 53.

Staff agrees with Respondents that the Infineon [redacted] products are not representative of the [redacted] products. Staff states that this lack of representativeness is shown, *inter alia*, by Dr. Sechen's infringement analyses, which provided measurements for the "part" at issue which were two to three times larger for the [redacted] products than for the [redacted] products. SIB at 85. Staff states that Dr. Sechen's statements that use of the [redacted] will lead to identical structures in the two products fail to take into account the different processes used, as explained by Respondents' expert Dr. Bravman. Staff argues that a likely explanation for the discrepancies between the Tyndall [redacted] images and the Infineon [redacted] images is the lower resolution of the Tyndall images, as well as certain flaws with the Tyndall images. *Id.* at 87-90. Staff argues that "Dr. Sechen's implication that the images from Infineon are untrustworthy (because Infineon has an interest in the case) is speculative." *Id.* at 90; *see also* SRB at 27-28.

Upon review of the evidence and the parties submissions, the undersigned finds that Arigna has not shown, by a preponderance of the evidence, that the Infineon [redacted] products are representative of the Infineon [redacted] products.

First, the TEM images produced by Infineon indicate that there are material differences between the [redacted] and [redacted] products that are relevant to the disputed limitations. It is undisputed that these images show significant differences, including a [redacted] in the conductive portion in the [redacted] products. *See* CIB at 150 (noting parts in the [redacted] wafer products referred to, *inter alia*, as [redacted]); RIB at 112-114 (discussing [redacted] of trench contact in devices made from [redacted] wafers); SIB at 84-85 (discussing [redacted] in [redacted]

wafer images); Tr. (Bravman) at 748:21-751:751:6. This different shape is apparent in -Dr. Sechen's own demonstratives of the Infineon [redacted] product and [redacted] product images. *Compare* CDX-001C-195 (showing CX-01055C, an "Infineon [redacted]" Image"); CDX-001C-196 (showing CX-01044C, an "Infineon [redacted]" Image"); Tr. (Sechen) at 358:20-360:12. This differing structure is material to the assessment of whether there may be the claimed "conductive portion . . . being in contact with a upper surface of said source layer" and "dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10 nm or more and 40 nm or less." '082 patent, claim 8; *see* Tr. (Sechen) at 540:7-540:19; RDX-107A; RDX-107B; SIB at 85 (discussing Dr. Sechen's differing analyses for the [redacted] and [redacted] products).

Second, Arigna's arguments for discounting the Infineon images are inadequate. Arigna relies heavily on the fact that [redacted] are used for both the [redacted] and [redacted] products, and suggests that any results showing different outcomes should therefore be viewed with skepticism and/or ignored. However, different machines and processes were used for the [redacted] and [redacted] products, and Dr. Bravman testified that these differing processes can impact structures of the chip. *See* JX-00020C ([redacted] at 62:18-63:9; Tr. (Bravman) at 747:1-749:4. Although Dr. Sechen testified that there is a "one-to-one correspondence" between the [redacted] and the cross-section, Dr. Sechen did not provide any analysis showing whether or how the features of interest for the disputed limitations in either the [redacted] or [redacted] products map onto (or fail to map onto) the [redacted], instead relying only on cross-sectional images for his infringement analysis—and he further admitted that assessment of claim 8's disputed limitations must be

ascertained based on a cross-sectional view. *See* Tr. (Sechen) at 595:7-12; SIB at 86 n.26.[55] Moreover, Arigna provided no specific evidence indicating that the Infineon images showing clear differences between the [redacted] and [redacted] products are unreliable, or contradicting Mr. [redacted] testimony regarding the way the Infineon images were created. *See* Tr. (Sechen) at 466:4-24; SIB at 90.[56]

Further, Arigna does not persuasively controvert Dr. Bravman's testimony indicating that the Tyndall [redacted] SEM image relied upon by Arigna (CX-00178C/RX-2672)[57] to show representativeness is unreliable. Among other issues identified, Dr. Bravman testified that, based on the lack of a [redacted] during sample preparation, this image exhibits "curtaining" which distorted the sample and created imaging artifacts. *See* Tr. (Bravman) at 822:1-825:12; RDX-0003C.89-92; *see also* Tr. (Sechen) at 485:17-486:9 (agreeing that he learned that [redacted] and so "some vertical artifacts ('curtains') were present in the cross-sections"). Dr. Bravman also showed other Tyndall images that he testified lacked the structure identified by Dr. Sechen in CX-00178C. *See* Tr. (Bravman) at 754:2-755:3 and RDX-0003C.46 (testifying that RX-2685C image from Tyndall does not have [redacted] present in [redacted] product image); RIB at 118; Tr. (Bravman) at 824:15-825:9 and RDX-

[55] In addition, Dr. Sechen testified that based on commonality of "the most [redacted]," he would expect the dimensions of the "all the features, all the key features" to be "approximately the same." Tr. (Sechen) at 532:1-5. Dr. Sechen did not provide testimony establishing that the particular [redacted] at issue in this investigation are "key features."

[56] Dr. Sechen testified that an image may "be rotated a bit" but acknowledged that he had "no evidence to prove that." Tr. (Sechen) at 355:18-356:1. This speculative testimony is not probative support for Arigna's position.

[57] CX-00178C and RX-2672 contain the same image. *See* RIB at 101, 102 n.17. Dr. Bravman testified that the images shown on RDX-0003.91 (RX-2691C, RX-2689C, RX-2690C, RX-2687C, RX-2672, and RX-2688C) are different magnifications of the image. Tr. (Bravman) at 823:12-25; RIB at 102-103.

0003C.92 (testifying that other Tyndall SEM images do not have [redacted] and show [redacted]); RIB at 104 n.18. Dr. Bravman further testified that measurements taken by Dr. Sechen using the Tyndall image were problematic because the low resolution provided by SEMs was insufficient for discerning the relevant structures properly. *See* Tr. (Bravman) at 818:12-821:1; RDX-0003C.87-88; RIB at 101-106.[58] Arigna did not identify any testimony or evidence substantively addressing these issues with the Tyndall image. *See* CIB at 132-132; CRB at 99-103.

Taken as a whole, the evidence does not show that the Tyndall image is more reliable than the Infineon images for assessing the accused chips from [redacted] wafers or for comparing them to chips from [redacted] wafers; rather, the evidence indicates that the Tyndall image is not reliable. As a result, given the material differences between the [redacted] and [redacted] products demonstrated by the Infineon images (discussed in the element-by-element analysis below), the evidence fails to show, by a preponderance, that EDT2 and TRENCHSTOP 5 chips from [redacted] wafers are representative of those from [redacted] wafers.

3. Element-by-Element Analysis (Claim 8)

With respect to infringement by the accused chips, and as discussed above, Arigna accuses certain Infineon EDT2 and TRENCHSTOP 5 chips of infringing claim 8 of the '867 patent. CIB at 134-67; CRB at 103-29; Tr. (Sechen) at 313:12-363:9. Respondents argue that the EDT2 and TRENCHSTOP 5 chips do not meet the "upper surface" and "dimension of a part"

[58] Dr. Bravman testified (as Dr. Sechen did not dispute) that TEM offers significantly higher resolution than SEM images. *See* Tr. (Bravman) at 761:20-23 (TEM resolution is typically 10 to 50 times improved over SEMs); Tr. (Sechen) at 464:16-25 (generally agreeing that "TEM is certainly higher resolution and better than SEM").

limitations of claim 8, relying on the testimony of Dr. Bravman. RIB at 119-47; RRB at 56-75; Tr. (Bravman) at 756:16-834:9. Staff agrees with Respondents that the EDT2 and TRENCHSTOP 5 chips do not infringe claim 8 of the '867 patent. SIB at 91-104; SRB at 29-33.

With respect to Respondents' general arguments about the credibility of Dr. Sechen's testimony, *see* RIB at 92-99, the undersigned finds that some of Dr. Sechen's analysis is not reliable, as discussed below in the context of the "dimension of a part" limitation. The undersigned does not agree with Respondents that Dr. Sechen's testimony should be broadly discounted, however.[59]

Claim 8 is addressed on a limitation-by-limitation basis below. For the reasons discussed, the evidence does not show, by a preponderance, that the accused Infineon EDT2 and TRENCHSTOP 5 chips made from [redacted] wafers infringe claim 8. Thus there is no infringement by any imported products.[60]

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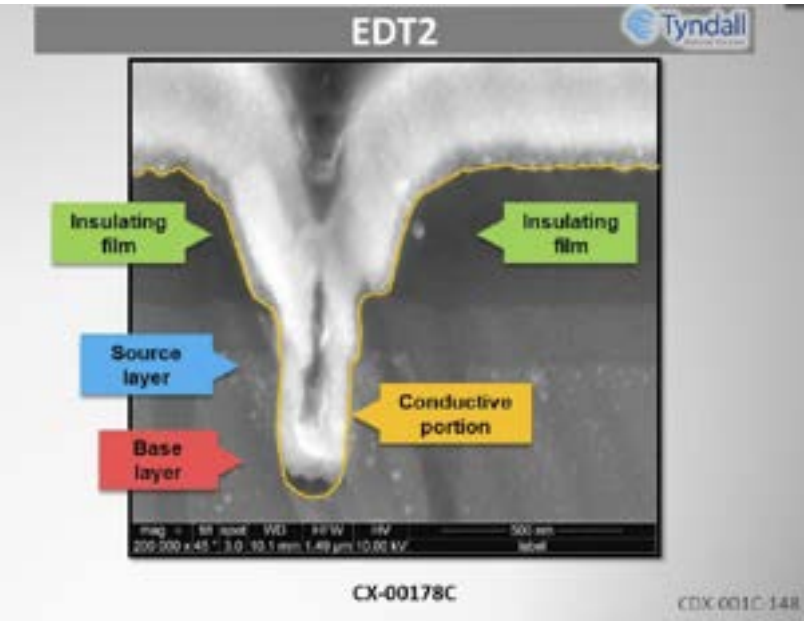
[59] In its reply brief, Arigna directly addresses the arguments raised by Respondents regarding Dr. Sechen's credibility. CRB at 78-86. On May 13, 2022, Respondents filed a motion (1267-050) to strike, *inter alia*, a portion of these arguments and to strike Exhibit A to Arigna's reply post-hearing brief (a copy of Dr. Sechen's expert report). *See supra*, n.8. Arigna filed a response in opposition to the motion on May 25, 2022. Staff filed a response in support of the motion on May 25, 2022. In consideration of the motion and responses thereto, the undersigned agrees with Respondents and Staff that Arigna's citation to Dr. Sechen's expert report on this issue should not be permitted, because the expert report is not in evidence. Arigna argues that it needs to cite Dr. Sechen's expert report to rebut Respondents' contention that Dr. Sechen's testimony at hearing was inconsistent with his expert report, but if Arigna wanted to rehabilitate Dr. Sechen's testimony, they could have addressed this issue in re-direct examination. Having failed to address this issue at hearing, Arigna cannot supplement the record by citing disclosures from Dr. Sechen's expert report in its reply post-hearing brief. Accordingly, the motion (1267-050) is hereby GRANTED-IN-PART with respect to the portion of Arigna's reply post-hearing brief that cites Dr. Sechen's expert report to discuss his identification of the "conductive portion" in the accused products. *See* CRB at 82-84 (citing Exhibit A). As discussed *supra*, n.8, the motion is DENIED-IN-PART as moot with respect to Exhibit A, which the parties agree is not in evidence.

[60] Because it is irrelevant to a finding of violation, Arigna's alleged evidence of infringement for products made on [redacted] wafers is not addressed in this determination. *See Certain Integrated Circuit Telecommunication Chips and Prods. Containing Same Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 24-25, USITC Pub. No. 2670, 1993 WL 13033517, at *20 (Aug. 1993) ("Importation (or at least a sale for importation) of the infringing articles is an essential element of a

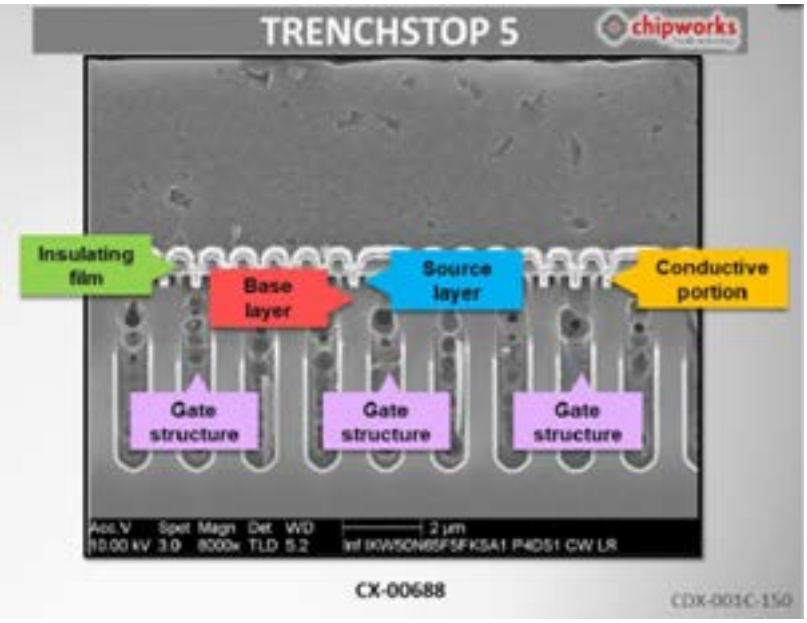
a. "A semiconductor device, comprising"

Dr. Sechen submits that the Infineon EDT2 and TRENCHSTOP 5 chips are insulated gate bipolar transistors ("IGBTs"). Tr. (Sechen) at 313:12-317:17; CDX-001C-147-150; CX-01151 (EDT2 datasheet); CX-01128 (TRENCHSTOP 5 datasheet). He identifies a cross-sectional image of an EDT2 chip showing various layers. Tr. (Sechen) at 314:25-16.



CDX-001C-148; CX-00178C. Dr. Sechen identifies a cross-sectional image of a TRENCHSTOP 5 chip showing various layers. Tr. (Sechen) at 315:25-316:16.

violation of section 337."). As discussed above, Arigna has not shown importation of [redacted] products or that [redacted] products are representative of [redacted] products for purposes of the disputed limitations of claim 8.



CDX-001C-150; CX-00688. There is no dispute that the Infineon EDT2 and TRENCHSTOP 5 chips at issue are semiconductor devices. *See* CIB at 132-33.[61]

b. "a base layer having a first conductivity type"

Dr. Sechen identifies a base layer composed of P-type doped silicon that can be seen in cross-sectional images of an EDT2 chip. Tr. (Sechen) at 314:25-16, 318:21-319:19; CDX-001C-148; CDX-001C-153-154; CX-00175C at 15; CX-00178C. Dr. Sechen identifies a similar P-type base layer in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 315:25-316:16, 320:10-321:3; CDX-001C-150; CDX-001C-155-156; CX-01031C at 66; CX-00688C. There is no dispute that the "base layer" limitation is met by the EDT2 and TRENCHSTOP 5 chips at issue. *See* CIB at 136-37.

[61] Dr. Sechen relies in part on the Tyndall EDT2 and Chipworks TRENCHSTOP 5 images for showing that the products at issue meet the undisputed limitations of claim 8 even though the Chipworks image relates to an [redacted] wafer product and the Tyndall image is unreliable for purposes of determining the disputed limitations at issue. *See, e.g.*, CIB at 135, 140; discussion *supra*. Given that the representativeness issue relates to the structures involved in the disputed limitations, however, this evidence (combined with the other evidence presented) appears sufficient for purposes of the undisputed limitations.

c. "a source layer formed on said base layer and having a second conductivity type"

Dr. Sechen identifies a source layer composed N-type silicon that can be seen in cross-sectional images of an EDT2 chip. Tr. (Sechen) at 314:25-16, 318:21-320:2; CDX-001C-148; CX-00178C. Dr. Sechen explains that P-type and N-type are two different conductivity types. Tr. (Sechen) at 320:3-9. Dr. Sechen identifies a similar N-type source layer in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 315:25-316:16, 320:10-321:3; CDX-001C-150 (CX-00688C). There is no dispute that the "source layer" limitation is met by the EDT2 and TRENCHSTOP 5 chips at issue. *See* CIB at 138-39.

d. "an insulating film formed on said source layer"

Dr. Sechen identifies an oxide insulating film that can be seen in cross-sectional images of an EDT2 chip. Tr. (Sechen) at 314:25-16; CDX-001C-148 (CX-00178C). Dr. Sechen identifies a similar insulating film in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 315:25-316:16; CDX-001C-150; CX-00688C. There is no dispute that the "insulating film" limitation is met by the EDT2 and TRENCHSTOP 5 chips at issue. *See* CIB at 139-14.

e. "a plurality of gate structures penetrating said base layer"

Dr. Sechen offered his opinion at the hearing that the EDT2 and TRENCHSTOP 5 chips have a plurality of gate structures penetrating the base layer. Tr. (Sechen) at 322:6-21; CDX-001C.165. Dr. Sechen specifically identifies gate structures in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 315:25-316:16; CDX-001C-150; CX-00688C. There is no dispute that the "plurality of gate structures" limitation is met by the EDT2 and TRENCHSTOP 5 chips at issue. *See* CIB at 139-14.

f. "a conductive portion penetrating said insulating film and said source layer, being in contact with an upper surface of said source layer, and electrically connected to said source layer and said base layer"

This limitation is disputed. Dr. Sechen identifies a [redacted] in cross-sectional images of trench contacts in an EDT2 chip representing "a conductive portion penetrating the insulating film." Tr. (Sechen) at 323:15-324:16; CDX-001C-171; CX-01052C. [62] He identifies a similar barrier layer in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 324:20-325:18; CDX-001C-174; CX-01077C. He explains that in both the EDT2 and TRENCHSTOP 5 chips, the barrier layer is electrically connected to the source layer and the base layer. Tr. (Sechen) at 325:19-326:10, 327:3-17; CDX-001C-158. Dr. Sechen also cites the testimony of Infineon representative [redacted] who testified that the [redacted] Tr. (Sechen) at 326:12-327:2; CDX-001C-176 (quoting JX-00020C ([redacted] Tr.) at 182:10-12).

With respect to the claim limitation requiring that the conductive portion is "in contact with an upper surface of said source layer," Dr. Sechen identifies part of the source layer that he states is angled downward near the gate structure. Tr. (Sechen) at 333:4-336:16; CDX-001C-183; CX-00178C. He explains that "the conductive portion rests on the source layer at an angled way." Tr. (Sechen) at 334:15-24. In his opinion, this is the "upper surface" of the source layer because, "[w]hen viewed from the top . . . that silicon surface is the first thing you see." *Id*. at 334:25-335:13.

[62] Respondents argue that Arigna waived its infringement theory based on a [redacted] because Dr. Sechen did not identify this layer in his expert report. RRB at 56-57. This waiver argument will not be considered, however, because Respondents failed to raise any objection to Dr. Sechen's at hearing where he clearly identified the [redacted]. *See* Tr. (Sechen) at 323:15-324:16.

Dr. Sechen relies on different cross-sectional images for the two relevant categories of products, which are addressed below. Respondents dispute that this claim limitation is met, also providing separate analyses for the two categories of products. *See* RIB at 124-144.[63]

(i). **EDT2 products from [redacted] wafers**

Dr. Sechen identifies an alleged "upper surface" in contact with the source layer in cross-sectional images produced by Infineon for EDT2 products manufactured on [redacted] wafers. Tr. (Sechen) at 343:22-348:5.[64]

[redacted]

CDX-001C-187 (citing CX-01039C; CX-01040C); *see also* CDX-001C-188 (citing CX-01048C; CX-01051C). He identifies the two ends of the relevant part starting from "a vertical wall of the boundary between the [redacted]

[63] The parties separately addressed products made on [redacted] wafers and [redacted] wafers. As discussed *supra*., n.60, only the evidence regarding products made on [redacted] wafers is addressed herein.

[64] Dr. Sechen also relied on a Tyndall image for an EDT2 product manufactured on a [redacted] wafer, Tr. (Sechen) at 332:2-335:13; CDX-001C-183 (CX-00178C), but as discussed *supra*, his analysis of this image is unreliable.

[redacted] Tr. (Sechen) at 344:3-12. Arigna argues that these [redacted] are the "upper surface" of the source layer in accordance with this term's plain and ordinary meaning. CIB at 119-123. Arigna further argues that such surfaces are consistent with the teaching in the specification of the '867 patent explaining that the purpose of the "upper surface "is to absorb the stress that in the manufacturing process. *See* CIB at 123; '867 patent at 10:41-45 ("[T]he stress that is generated in wire bonding for the source electrode 9 is absorbed by the upper surface of the source layer 4."). Dr. Sechen submits that these [redacted] represent "[t]he portion of the source upon which the conductive portion is resting." Tr. (Sechen) at 345:14-19.

Respondents dispute Dr. Sechen's identification of an "upper surface" in Infineon's cross-sectional images of EDT2 products made on [redacted] wafers, relying on Dr. Bravman's analysis. RIB at 124-33; Tr. (Bravman) at 761:25-769:13, 771:16-805:9. Dr. Bravman submits that the "upper surface" of the silicon source layer is the top-most surface, [redacted] cross-sectional images adjacent to the trench contact. Tr. (Bravman) at 803:1-24; RDX-0003C.62. To support his interpretation of "upper surface," Dr. Bravman explained that the specification of the '867 patent describes a manufacturing process that would create a "stair-step structure," where "the upper surface remains the upper surface." Tr. (Bravman) at 757:13-759:8; RDX-0003C.50-53; *see* '867 patent at 10:21-40 ("[I]n this preferred embodiment, part of the conductive portion 8 is in contact with the upper surface of the source layer 4"). Respondents further contend that Arigna previously agreed that the "upper surface" is the top-most surface and that lateral surfaces would not be the "upper surface" even if they deviated from a vertical position. *Id*. at 120-21.

Even under Dr. Sechen's interpretation of "upper surface," Respondents dispute whether the [redacted] identified as the "conductive portion" by Dr. Sechen is "in contact with" the "upper surface" of the silicon source layer. RIB at 138-41; RRB at 56-57. According to Dr. Bravman, the "upper surface" identified by Dr. Sechen in contact with the [redacted] "is not the true boundary between the silicon and the conducting portion" but represents "parts of the [redacted] structure which, again, is [redacted]." Tr. (Bravman) at 764:15-765:22.

RDX-0045C (annotated by Dr. Bravman).

Respondents further argue that even if the features identified by Dr. Sechen were a surface of the silicon source layer in contact with the conductive [redacted], it would not meet Dr. Sechen's own definition of "upper surface," which requires a surface that is facing upward

and visible from a top view. RIB at 131-33. A significant part of Dr. Sechen's "upper surface" that is in contact with the [redacted] would not be visible from a top view—it would be blocked in part [redacted]. *See* Tr. (Bravman) at 816:17-817:8 ("If I look down that pipe, what I would see is [redacted] hitting the top surface of the silicon."). Staff agrees with Respondents that Dr. Sechen has identified a lateral surface of the silicon source layer rather than an "upper surface." SIB at 92-96.

In consideration of the parties' arguments, the undersigned agrees with Respondents and Staff that Arigna has failed to identify, by a preponderance of the evidence, an "upper surface" of the source layer in the EDT2 products manufacture on [redacted] wafers that meets the limitations of the "conductive portion" limitation. Although the undersigned agrees with Arigna that an [redacted] can be an "upper surface" of the source layer in accordance with the claim language, the "upper surface" identified by Dr. Sechen in the Infineon cross-sectional images does not meet his own stated criteria—because the [redacted] from the trench, there is a portion of Dr. Sechen's "upper surface" that would not be visible from a top view.

The undersigned further agrees with Respondents and Staff that Dr. Sechen failed to apply any reliable methodology for identifying the portion of the silicon source layer that is in contact with the barrier layer. As Staff notes, Dr. Sechen did not annotate any of the Infineon [redacted] images to specifically identify what he claimed to be the relevant portion of the "upper surface." SIB at 101-02. The undersigned credits Dr. Bravman's testimony that the area where the trench contact meets the silicon source layer [redacted], Tr. (Bravman) at 764:15-765:22, and the undersigned thus finds that Dr. Sechen's analysis of [redacted] on the cross-sectional images is insufficient to reliably identify where the silicon is in

contact with the barrier layer. *See, e.g.,* Tr. (Sechen) at 346:18-24; RIB at 128-130. Accordingly, the undersigned finds that Arigna has failed to carry its burden to prove infringement of the limitation requiring the conductive portion to be "in contact with an upper surface of said source layer" with respect to the EDT2 products made on [redacted] wafers.

(ii). **TRENCHSTOP 5 products from [redacted] wafers**

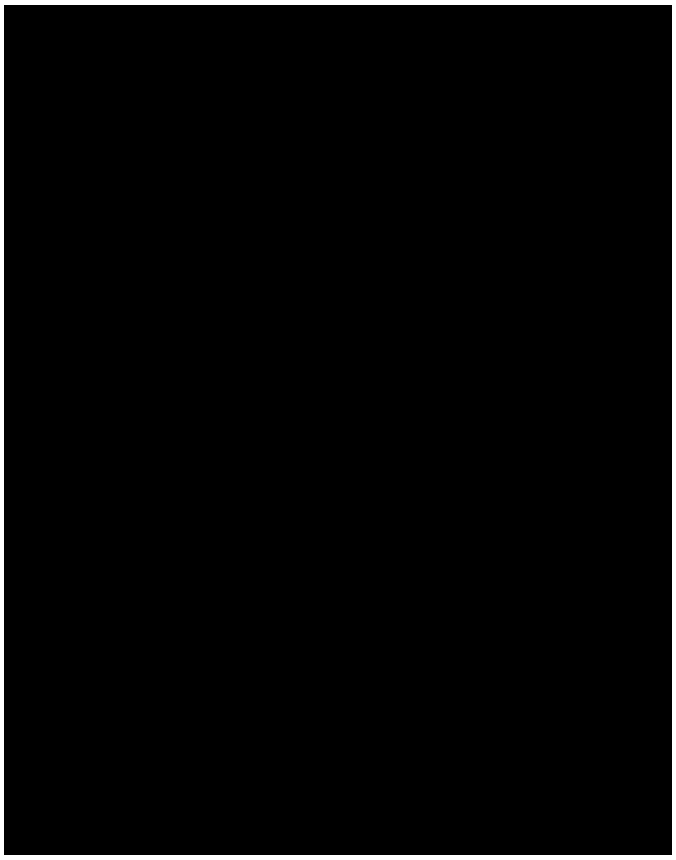
Dr. Sechen identifies an alleged "upper surface" in contact with the source layer in cross-sectional images produced by Infineon for TRENCHSTOP 5 products manufactured on [redacted] wafers. Tr. (Sechen) at 353:16-355:8.

CDX-001C-193 (citing CX-01068C); *see also* CDX-001C-192 (citing CX-1063C). He explains that "[t]he left vertical line is where [redacted]" Tr. (Sechen) at 354:23-355:4.

Respondents dispute Dr. Sechen's identification of an "upper surface" in Infineon's cross-sectional images of TRENCHSTOP 5 products made on [redacted] wafers, making similar

arguments to those addressed above in the context of the EDT2 products. RIB at 133-38. For the TRENCHSTOP 5 products, Dr. Bravman reviewed Infineon cross-sectional images and found that the contact between the silicon source layer and the [redacted], with no meaningful contact with an "upper surface" of the source layer. Tr. (Bravman) at 805:10-808:23.

RDX-0003C.68 (CX-00143C.12); RDX-0003C.67 (CX-00143C.13). Dr. Bravman further identifies an EFTEM image showing [redacted] at the trench contact. Tr. (Bravman) at 807:15-808:16.



RDX-0003C.71 (CX-00143C.21). Staff agrees with Respondents that the evidence does not show that the TRENCHSTOP 5 products made on [redacted] wafers meet this limitation. SIB At 103.

For the same reasons discussed above in the context of the EDT2 product, the undersigned finds that Arigna has failed to carry its burden to prove infringement of the limitation requiring the conductive portion to be "in contact with an upper surface of said source layer" with respect to the imported TRENCHSTOP 5 products. The Infineon cross-sectional images for these products show [redacted], and it is unclear where precisely the silicon is in contact with the [redacted], if any, would be visible from a top view. As discussed above, Dr. Sechen failed to apply any reliable methodology for identifying an "upper surface" of the source layer that is in contact with the [redacted].

g. "a source electrode formed on said insulating film and electrically connected to said conductive portion"

Dr. Sechen offered his opinion at the hearing that an aluminum source electrode is formed on the oxide insulating film and is electrically connected to the barrier layer in the EDT2 and TRENCHSTOP 5. Tr. (Sechen) at 328:28-330:4; CDX-001C.165. Dr. Sechen specifically identifies gate structures in cross-sectional images of a TRENCHSTOP 5 chip. Tr. (Sechen) at 315:25-316:16; CDX-001C-178 (CX-00178C). There is no dispute that the "source electrode" limitation is met by the EDT2 and TRENCHSTOP 5 chips. *See* CIB at 152-54.

h. "wherein a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10nm or more and 40nm or less"

Dr. Sechen analyzed several cross-sectional images to measure the horizontal width of the asserted "upper surface" of the source layer that is in contact with the barrier layer. Tr. (Sechen) at 330:5-355:8. Dr. Sechen first employs a methodology for measuring the relevant width that is based on the specification of the '867 patent, measuring the full width of the conductive portion above and below the contact with the source layer, subtracting these two widths and dividing by two. *Id*. at 332:3-334:2; CDX-001C-183; *see* '867 patent at 9:66-10:0, Fig. 7. Using a Tyndall image of a [redacted] EDT2 product, Dr. Sechen measures the relevant dimension to be 27 nanometers. Tr. (Sechen) at 332:19-334:2; CDX-001C-13 (CX-00178C).[65] He performs the same measurement using a Chipworks image of an [redacted] TRENCHSTOP 5 product, measuring the relevant dimension to be 17.5 nanometers. Tr. (Sechen) at 348:6-349:15; CDX-001C-189 (CX-00689C).[66] Dr. Sechen also identifies and measures the relevant

[65] As discussed *supra*, this image is unreliable with respect to the disputed claim limitations.

[66] As discussed *supra*, n.60, this infringement evidence for a product made on an [redacted] wafer is irrelevant.

dimension on cross-sectional images produced by Infineon for the imported EDT2 and TRENCHSTOP 5 products, as discussed below:

(i). **EDT2 products from [redacted] wafers**

As discussed above, Dr. Sechen identifies an alleged "upper surface" in contact with the source layer in cross-sectional images produced by Infineon for EDT2 products manufactured on [redacted] wafers. Tr. (Sechen) at 343:22-348:5. In one image of a trench contact, he measured the horizontal width of this part to be [redacted]. *Id*. at 344:24-355:2; CX-01039C. In another image, he measured the width to be [redacted]. Tr. (Sechen) at 346:1-4; CX-01040C.

CDX-001C-187. He analyzes two other images of EDT2 products manufactured on [redacted] wafers, measuring dimensions of [redacted]. Tr. (Sechen) at 346:5-348:19; CDX-001C-188 (citing CX-01048C; CX-1051C).

As discussed above in the context of the "upper surface" limitation, the undersigned agrees with Respondents and Staff that Dr. Sechen's identification of the "upper surface" in contact with the silicon source layer in the Infineon images of products from [redacted] wafers is

unreliable. Dr. Sechen's measurement of the alleged "dimension of a part" is also unreliable, as demonstrated by Dr. Sechen's preparation of two sets of demonstratives for the hearing regarding this dimension. *See* Tr. (Sechen) at 490:18-491:15. In an alternative version of CDX-001C-187, Dr. Sechen measured the relevant dimension on the left image to be [redacted]. Tr. (Sechen) at 498:20-500:20. 501:15-502:7; RDX-0103C. He was unable to explain the discrepancy between the two measurements. *Id*. The difference between these two measurements raises significant reliability issues for the infringement analysis; among other things it shows that Dr. Sechen's measurements can vary by as much as [redacted] for the same dimension, and one of the measurements [redacted] from the low end of the claimed range (10-40nm). Accordingly, the undersigned finds that Dr. Sechen has failed to reliably measure the claimed "dimension of part," and Arigna has failed to show this limitation is met for the imported EDT2 products.

(ii). **TRENCHSTOP 5 products from [redacted] wafers**

As discussed above, Dr. Sechen identifies an alleged "upper surface" in contact with the source layer in cross-sectional images produced by Infineon for EDT2 products manufactured on [redacted] wafers. Tr. (Sechen) at 353:16-355:8. In one image of a trench contact, he measured the horizontal width of this part to be [redacted]. *Id*. at 354:12-14; CDX-001C-192 (citing CX-1063C). In another image, he measured the width to be [redacted]. Tr. (Sechen) at 355:5-8.

CDX-001C-193 (citing CX-01068C).

As discussed above in the context of the "conductive portion" limitation, the undersigned agrees with Respondents and Staff that Dr. Sechen's identification of the "upper surface" in contact with the silicon source layer in the Infineon images of products from [redacted] wafers is unreliable. Dr. Sechen's measurement of his alleged "dimension of a part" is also unreliable, as demonstrated by Dr. Sechen's preparation of two sets of demonstratives for the hearing regarding this dimension. *See* Tr. (Sechen) at 490:18-491:15. In an alternative version of CDX-001C-192, Dr. Sechen measured the relevant dimension on the left image to be [redacted]. Tr. (Sechen) at 504:10-505:5; RDX-0105C. He was unable to explain the discrepancy between the two measurements. *Id*. The difference between these two measurements is significant to the infringement analysis; among other things it shows that Dr. Sechen's measurements can vary by as much as [redacted] for the same dimension, and one of the measurements [redacted] from the low end of the claimed range (10-40nm). Accordingly, the undersigned finds that Dr. Sechen has failed to reliably measure the claimed

"dimension of part," and Arigna has failed to show this limitation is met for the imported TRENCHSTOP 5 products.

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For the reasons discussed above, the undersigned finds that Arigna has not shown, by a preponderance of the evidence, that any accused imported products meet the limitations of claim 8 of the '867 patent. Accordingly, the undersigned finds no infringement of claim 8 of the '867 patent.

G. Domestic Industry

The asserted domestic industry products, for purposes of the '867 patent, are Microchip's [redacted] CIB at 104. Both the [redacted] are "Trench FET devices." *See* JX-00016C (Microchip) at 17:3-25.[67] According to the Microchip witness, these are products in development that are intended to be integrated into [redacted] (MCM). JX-00016C (Microchip) at 26:16-20 ([redacted] *id.* at 41:12-21 [redacted]; *id.* at 43:20-23 [redacted] The [redacted] is an "8k" FET, while the [redacted] is a "10k" FET. *See* JX-00016C (Microchip) at 31:23-32:1; CRB at 131; SIB at 106.[68]

1. Domestic Industry Articles

As an initial matter, the parties dispute whether actual "articles" exist. To show that a domestic industry exists, it is necessary to show the existence of "articles" protected by the

[67] The term "FET" refers to "field effect transistor," which is "a three-terminal device that turns on or off during certain conditions applied to one of the terminals." *See* JX-00016C at 17:18-22, 39:24-40:10. A "trench" FET is a type of FET "typically used for higher power FET devices." *Id.* at 39:24-40:2.

[68] The difference between an "8k" FET device and a "10k" FET device" relates the "breakdown voltage of the transistor." JX-00016C (Microchip) at 18:1-8. An 8k device "signifies an 80-volt breakdown voltage," while "10k signifies a 100-volt . . . breakdown voltage." *Id.*

patent. *See Microsoft Corp. v. Int'l Trade Comm'n*, 731 F.3d 1354 (Fed. Cir. 2013) ("[a] company seeking section 337 protection must . . . provide evidence that . . . relates to an actual article that practices the patent"); *Certain Thermoplastic-Encapsulated Electric Motors, Components thereof, and Products and Vehicles Containing the Same*, Inv. No. 337-TA-1073, Comm'n Op., 2019 WL 9596564, at *6 (Aug. 12, 2019) ("Both Federal Circuit law and Commission precedent require the existence of actual 'articles protected by the patent' in order to find that a domestic industry exists."). Such "articles" need not be commercial items, but can encompass "pre-commercial or non-commercial" items. *See Certain Non-Volatile Memory Devices and Prods. Containing Same*, Inv. No. 337-TA-1046, Comm'n Op., 2018 WL 6012622, at *25 (Oct. 26, 2018) ("The term 'article' on its own is sufficiently capacious to embrace pre-commercial or non-commercial items. And the fact that section 337 allows a complainant to establish a domestic industry based on an industry 'in the process of being established' strongly suggests that Congress did not envision commercialization as a prerequisite."); *Certain Strontium-Rubidium Radioisotope Infusion Systems, and Components Thereof Including Generators*, Inv. No. 337-TA-1110, Initial Determination, USITC Pub. No. 5025, 2020 WL 9312369, at *117. (Aug. 1, 2019) ("Other Commission decisions illustrate that commercial availability of a patented article in the United States is not necessary to show either that a domestic industry exists or . . . an industry in the process of being established.").

With respect to an industry "in the process of being established," the Commission has not determined "the circumstances, if any, in which a complainant can demonstrate a domestic

industry in the process of being established absent the existence of a protected article." 2019 WL 9596564, at *7.[69]

Here, while Arigna's expert, Dr. Sechen, provided testimony based on certain GDSII files associated with [redacted] and [redacted] *i.e.,* files used to create masks used during wafer production.[70] Respondents dispute whether these GDSII files have been used to create actual semiconductor devices.

Arigna contends that Microchip "has fabricated physical units of the [redacted] and [redacted] CIB at 167 (citing JX-00016C at 17:3-25, 20:22-24:13, and 59:8-61:15 as well as CX-0073C and CX-00076C); CRB at 130-131.[71] Arigna further argues that "Microchip will incorporate (and has already incorporated" the [redacted] and [redacted] in [redacted] that will be available for commercial sale beginning in third quarter of 2022." CIB at 168; *see also* CRB at 131.

Respondents argue, in opposition, that Arigna is relying on the GDSII files of [redacted] and [redacted] rather than the physical products themselves. RIB at 148. Respondents argue that Arigna relies on "[redacted]" to show that the [redacted] and [redacted] have been produced, but that this document "shows cross-sections for an

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[69] The Notice of Institution of Investigation encompasses both the existence of a domestic industry and a domestic industry in the process of being established. 86 *Fed. Reg.* 34042 (June 28, 2021).

[70] *See* JX-00016C (Jamarillo) at 15:7-18 (testifying that a "GDSII file is primarily used to generate the masks created and needed to process material and develop the production within a wafer application facility," and a "[m]ask is a physical piece of hardware that takes a pattern of each mask layer derived by the GDSII file and uses it in photolithography equipment inside of our fab").

[71] Arigna also contends that the [redacted] and [redacted] GDSII files represent the "physical piece of hardware" to fabricate the [redacted] and [redacted] Arigna acknowledges, however, that it "is not pointing to the mask sets as the physical products . . . Instead, Complainant is pointing to the devices made using those mask sets as the physical articles at issue." CRB at 130.

[redacted] of the [redacted] GDSII file." *Id.* at 148-49. Respondents state that "At best, the TEM images in CX-0073C may show cross-sections of an [redacted], but they do not provide evidence of a physical article for the [redacted]." *Id.* (emphasis in original). Respondents further argue that, while Arigna cites to CX-0076C as support for fabrication, Arigna does not identify any particular page citation, and that this document "relates to [redacted] of the relevant mask sets." *See* RRB at 75-76. Respondents argue that the Microchip testimony relied upon by Arigna "does not indicate the existence of a physical article," and only generally relates to incorporating "some form of Trench FET in MCMs" (RRB at 77). Regarding Arigna's planned commercial release and sales, Respondents argue that the evidence is "unduly speculative." RRB at 78. Respondents argue that this case is analogous to *Certain Thermoplastic-Encapsulated Electric Motors*, where "the Commission held that CAD (computer aided design) drawing fell far short" of showing an industry in the process of being established. *Id.* (citing Inv. No. 337-TA-1073, Comm'n Op., 2019 WL 9596564, at *8 (Aug. 12, 2019)).

Staff contends that "the evidence shows that the [redacted] and [redacted] are physical prototype articles, and thus, can form the basis for a domestic industry under the Commission's caselaw." SIB at 105. Staff argues that testimony of Microchip's representative (Mr. Jamarillo) sufficiently indicated fabrication of prototype devices. *Id.* at 105-106. Staff states that "[w]hether a physical article needs to exist for an industry in the process of being established is an issue that the Commission has yet to decide." SIB at 106 n.34. Staff contends that further support for the existence of physical articles is found in "FET Development Update" presentations at CX-0075C.0015 and CX-0076C.0056. *See* SIB at 106-107. Staff states that Microchip confirmed during discovery that the [redacted] of the GDSII files had been produced. SIB at 107 (citing CX-02382C).

Upon review of the parties' submissions and evidence, the undersigned finds that the evidence shows, by a preponderance, that there exist physical "articles" for purposes of assessing the technical prong of the domestic industry requirement. The evidence indicates that, as part of the development process, the GDSII files for the [redacted] and [redacted] are used to create actual devices. Microchip's witness Mr. Jamarillo referred in his deposition testimony to the [redacted] and [redacted] as "devices" that are made according to the GDSII files. *See* JX-00016C (Microchip) at 17:18-25 ("[redacted]."). He further referenced the process of fabricating actual devices [redacted]. *See id.* at 23:3-16 ([redacted]); *id.* at 174:12-24 [redacted] products). In addition, there is documentary evidence incorporated into Microchip presentations that indicates fabrication of both [redacted] and [redacted] devices. *See, e.g.*, CX-00076C.0056 (showing shipped "lot" of [redacted][72]; CX-00075C.0015 (showing "lots" of [redacted][73]; SIB at 106-07.

Respondents contend that this evidence is insufficient because the Microchip documents show evidence regarding [redacted] of the products. RIB at 148-149; RRB at 75-76. However, the documentary evidence and Mr. Jamarillo's testimony indicate that these mask sets,

[72] Mr. Jamarillo testified that this document, entitled "FET Development Update" and dated August 5, 2021 (ITC_INV_337-1267_MICROCHIP_0000170738), is a "FET development team update" presented "by an engineer at the fab." CX-00016C at 92:6-23.

[73] Mr. Jamarillo testified that this document, entitled "FET Development Update" and dated May 6, 2021 ((ITC_INV_337-1267_MICROCHIP_0000170600) is, like CX-00076C, an "update on the development progress of the 8k and 10k trench FETs."

as a general matter, are used to manufacture devices that are then tested as part of the research and development process. This evidence is sufficient to show, by a preponderance, the existence of physical "articles" made using the [redacted] and [redacted] mask sets (and corresponding GDSII files).[74]

2. Technical Prong

Dr. Sechen relied on GDSII files, cross-sectional images, and other documents from Microchip to show that each limitation of claim 4 is practiced by Microchip's Trench FET [redacted] and [redacted] products. Tr. (Sechen) at 364:7-388:23, 390:8-395:24. He submits that the [redacted] is "substantially identical to the [redacted] for the purposes of his analysis. *Id.* at 390:11-21. Respondents do not dispute the substance of Dr. Sechen's analysis except to challenge the sufficiency of the evidence presented at hearing—particularly with respect to the [redacted] product. RIB at 148-49; RRB at 79-80. Staff agrees with Arigna that the Trench FET [redacted] and [redacted] products have been shown to practice claim 4. SIB at 104-05. Based on the evidence discussed below, the undersigned finds that Dr. Sechen's analysis is sufficient to show, by a preponderance of the evidence, the practice of each limitation of claim 4 by the [redacted] and [redacted] products.

a. "A semiconductor device, comprising"

Dr. Sechen reviewed GDSII files and other design documents describing the [redacted] product, concluding that these documents describe a semiconductor device. Tr. (Sechen) at

[74] In addition, to the extent an existing "article" is not required for purposes of a domestic industry in the process of being established (*see* 2019 WL 9596564, at *7), the evidence shows, by a preponderance, that the GDSII files for the [redacted] and [redacted] devices will be incorporated into an "article" at least for research and development purposes. *See, e.g.*, CX-0016C (Microchip) at 174:17-24 [redacted]

368:10-371:12 (citing CX-00092C; CX-00073C; CPX-006C). Dr. Sechen reviewed similar documents with respect to the [redacted] product. Tr. (Sechen) at 390:25-391:9 (citing CPX-006C).

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] product are semiconductor devices.

b. "a base layer having a first conductivity type"

Dr. Sechen identified [redacted]. Tr. (Sechen) at 371:32-372:4; CPX-006C. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation. Tr. (Sechen) at 391:10-14; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain a base layer meeting this limitation.

c. "a source layer formed on said base layer and having a second conductivity type"

Dr. Sechen explains that a base layer needs to have different a conductivity type from a source layer for a device to function as an FET. Tr. (Sechen) at 372:19-373:2. He identifies [redacted] *Id.* at 373:23-374:11; CPX-006C. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation. Tr. (Sechen) at 391:15-18; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain a source layer formed on the base layer with a second conductivity type meeting this limitation.

d. "an insulating film formed on said source layer"

Dr. Sechen explains that an insulating layer is required for an FET device to work. Tr. (Sechen) at 374:12-20, 391:19-392:1. He identifies a cross-sectional image showing an

insulating film on the gate trenches of the [redacted] showing that this film is formed on the source layer. *Id*. at 374:21-376:10.

CDX-001C_TDI-216; CX-00073C. Arigna submits that a similar layer is necessarily present in the [redacted] device. CIB at 189-90.

Respondents argue that Dr. Sechen's testimony is insufficient to show that the [redacted] practices this limitation but cites no contrary evidence. RRB at 79-80. On this record, the undersigned finds that Arigna has met its burden to show that the [redacted] and the [redacted] contain an insulating film formed on the source layer meeting this limitation.

e. "a plurality of gate structures penetrating said base layer"

Dr. Sechen explains that an FET device would not work without gate structures penetrating the base layers. Tr. (Sechen) at 376:12-20. He identifies gate structures depicted in cross-sectional images of the [redacted] *Id*. at 376:21-377:4. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation. Tr. (Sechen) at 392:2-10; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain a plurality of gate structures penetrating the base layer meeting this limitation.

f. "a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer"

Dr. Sechen reviewed GDSII files for the [redacted] to [redacted]. Tr. (Sechen) at 378:13-380:13. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation, [redacted]. Tr. (Sechen) at 393:6-394:6; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain a plurality of conductive portions electrically connected to the source layer and base layer meeting this limitation.

g. "a source electrode formed on said insulating film and electrically connected to said conductive portions"

Dr. Sechen explains that an FET product would not be able to function without a source electrode electrically connected to the conductive portions. Tr. (Sechen) at 380:14-25. He also identifies [redacted]. *Id.* at 381:1-13; CX-00073C. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation, [redacted]. Tr. (Sechen) at 394:7-16; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain a source electrode electrically connected to said conductive portions meeting this limitation.

h. "said gate structures are formed in a stripe shape in plan view"

Dr. Sechen identifies [redacted]. Tr. (Sechen) at 381:19-382:8; CPX-006C. He explains that [redacted] that the GDSII file shows the design in a top-down view. *Id.* at 382:9-25. Dr. Sechen also reviewed GDSII files for the [redacted] with respect to this limitation, [redacted]. Tr. (Sechen) at 392:12-393:5; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain gate structures formed in a stripe shape meeting this limitation.

i. "parts in which said conductive portions are connected to said base layer are formed, in plan view, side by side in an island shape in a direction of said stripe shape of said gate structures with a distance from said gate structures between said gate structures"

Dr. Sechen identifies [redacted]. Tr. (Sechen) at 383:19-385:15; CPX-007C. He explains that [redacted] *Id.* at 383:24-385:9. With respect to the [redacted] Dr. Sechen identified [redacted] with the [redacted] *Id.* at 393:18-394:6; CIB at 192; CPX-006C.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] contain conductive portions between gate structures that are formed side by side in an island shape meeting this limitation.

j. "a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures in a region in which said conductive portions are not connected to said base layer is 0.36 μm or more"

Dr. Sechen measures a distance of [redacted] of the [redacted] Tr. (Sechen) at 385:22-386:22; CPX-007C. He explains that [redacted]. Tr. (Sechen) at 387:3-388:2. Dr. Sechen further cites a Microchip design document for the [redacted]. *Id.* at 388:3-12; CX-00092C. Reviewing GDSII files for the [redacted] Dr. Sechen measures a [redacted]. Tr. (Sechen) at 394:20-395:22.

Based on this unrebutted evidence, the undersigned finds that the [redacted] and the [redacted] have a dimension of a part between gate structures that is more than 0.36 microns.

For the reasons discussed above, the undersigned finds that the [redacted] and the [redacted] thus practice each limitation of claim 4 of the '867 patent.

3. Economic Prong

Arigna submits that Microchip's employment of labor and capital with respect to its [redacted] products shows that a domestic industry exists or is in the process of being established with respect to the '867 patent. CIB at 228-34; Tr. (Smith) at 641:5-650:10.

a. Identification and Allocation of Expenditures

Arigna identifies investments in the development of Microchip's [redacted] products as the relevant domestic industry for the [redacted] and [redacted] products. CIB at 229-33. Although Microchip began developing these products in [redacted], Microchip was not licensed to the '867 patent until [redacted]. *See* CX-00097C. Accordingly, Arigna has only counted Microchip's

expenditures from [redacted][75] *See Certain Fluidized Supporting Apparatus*, Inv. Nos. 337-TA-182/188, Comm'n Op., 1984 WL 63741, *6 (Oct. 1, 1984) (absent a license, a company is "nothing more than an infringer, which cannot be part of the industry").

To describe the domestic industry activities, Arigna relies on the testimony of Rudy Jaramillo, Microchip's Director of Design, Product, and Testing Engineering for Analog Power Interface Products ("APID"). JX-00016C (Jaramillo Tr.) at 13:5-14:23. Mr. Jaramillo explains that the [redacted] is [redacted] products in development. *Id.* at 31:1-22. The [redacted] is an [redacted], and Microchip is developing at least [redacted]. *Id.* at 31:23-32:14. The [redacted] are part of Microchip's overall development of [redacted] that are not [redacted]. *Id.* at 109:14-110:4. Mr. Jaramillo explains that [redacted]. *Id.* at 41:1-9, 43:20-44:19. He identifies [redacted]. *Id.* at 22:20-23:18, 47:2548:4, 69:20-72:22.[76]

[75] Respondents argue that counting expenditures through June 2021 improperly includes investments that were made after the complaint was filed in May 2021. RIB at 191-92 (citing *Certain Television Sets*, Inv. No. 337-TA-910, Comm'n Op. at 56-57 (limiting the consideration of post-complaint evidence to "[e]xtraordinary developments."). The undersigned agrees with Respondents that there is no basis for considering post-complaint expenditures in this investigation, but whether the June 2021 expenditures are counted or not has no impact on the determination herein with respect to the domestic industry. *See* SRB at 57-58.

[76] Mr. Jaramillo also identifies [redacted]. *See Id.* at 49:11-14, 72:23-73:3.

Mr. Jamarillo identifies [redacted] employees [redacted] who devote [redacted] of their time to [redacted] development and [redacted] employee who spends [redacted] of his time on [redacted] development. JX-00016C (Jaramillo Tr.) at 71:17-72:22. Mr. Smith determined that from January 2020 to June 2021, he could attribute [redacted] of these employees' salaries and benefits to [redacted] development. Tr. (Smith) at 644:1-25; CDX-002C.51 (citing CX-00077C; CX-00078C). Mr. Smith obtained information on Microchip's R&D expenditures on [redacted] technology from [redacted] and allocated [redacted] of this amount to [redacted] products, resulting in [redacted]. Tr. (Smith) at 644:13-645:13; CDX-002C.49; CDX-002C.51 (citing CX-00077C). He also obtained information regarding the staffing and fabrication expenditures at [redacted] related to [redacted] products from [redacted], totaling [redacted]. Tr. (Smith) at 645:1-13; CDX-002C.51 (citing CX-00077C). Recognizing that the relevant timeframe is [redacted], Mr. Smith prorated each of these amounts to calculate a total domestic [redacted] expenditure of approximately [redacted]. Tr. (Smith) at 645:14-24; CDX-002C.52.

[redacted]

CDX-002C.52 (Citing CX-00077C; CX-00078C; JX-00016C (Jaramillo Tr.)). As an alternative, recognizing that there are at least [redacted] products in development other than the [redacted] and [redacted] Mr. Smith counted [redacted] of these expenditures, leaving approximately

[redacted] in domestic industry investments, which he described as "an extremely conservative" estimate. Tr. (Smith) at 645:25-646:25; CDX-002C.53. Mr. Smith maintains, however, that the [redacted] estimate is "a more appropriate figure." Tr. (Smith) at 683:24-684:6.

Respondents argue that the expenditures identified by Mr. Smith are overstated, especially with respect to the [redacted]. RIB at 189-91; RRB at 108-09. Respondents submit that Mr. Smith's alternative estimate of [redacted] is more accurate than his [redacted] estimate, because it includes the necessary step of allocating Microchip's expenditures to account for the fact that the [redacted] and [redacted] are [redacted] in development. *See* Tr. (Reed) at 956:1-958:4. Respondents further argue that Mr. Smith failed to properly allocate Microchip's labor expenditures to account for work on both [redacted]. RIB at 190; *see* Tr. (Reed) at 960:1-13. According to Mr. Reed, a proper allocation of Microchip's expenditures would estimate investments of only [redacted] attributable to the [redacted] and [redacted] Tr. (Reed) at 960:14-961:1; RDX-0002C.15.

Staff agrees with Respondents that Mr. Smith's alternative allocation is the more reliable estimate. SRB at 56. Staff does not agree with Respondents that any further allocation of labor expenditures is necessary, however, citing testimony from Mr. Jaramillo showing that it was likely that [redacted]. *Id*. at 56-57 (citing JX-00016C (Jaramillo Tr.) at 71:17-72:10, 217:22-218:16).

In consideration of the parties' arguments, the undersigned agrees with Staff that Mr. Smith's [redacted] estimate is the best estimate of domestic industry expenditures in the record. *See* Tr. (Smith) at 645:25-646:25; CDX-002C.53. Mr. Smith's accounting of labor expenditures for [redacted] is supported by Mr. Jaramillo's testimony, and there is no dispute with respect to his allocation of expenditures for [redacted] or his identification of

[redacted]. *See* SRB at 56-57. The undersigned agrees with Respondents and Staff that Mr. Smith's "alternative" allocation is necessary to exclude investments in [redacted] that have not been shown to practice any claim of the '867 patent. *See Certain Subsea Telecommunication Systems*, Inv. No. 337-TA-1098, Comm'n Op. at 41-47, EDIS Doc. ID 691678 (Oct. 21, 2019) (finding that the domestic industry is defined by the patented article, and complainants must "allocate expenses to account for non-domestic industry articles that do not practice the patent."). The undersigned recognizes that Mr. Smith's [redacted] estimate is not a precise accounting, and it is not clear whether this estimate understates or overstates the expenditures attributable to the [redacted] and [redacted] because there is no evidence that compares the work performed on the [redacted] and [redacted] with [redacted]. Nevertheless, this is likely the best estimate that can be made on this record, and the undersigned finds that Mr. Smith's methodology (applying his alternative allocation) is sufficiently reliable for this case.

b. Significance

Arigna submits that Microchip's investments in labor and capital are significant based on the absolute value of the investment in one year [redacted] and because the development of [redacted] technology represents [redacted] CIB at 233-34. Arigna further submits that the investments are qualitatively significant to Microchip because [redacted]. *Id*. (citing JX-00016C (Jaramillo Tr.) at 47:25-49:7, 89:16-89:19).

Respondents argue that Arigna has failed to place its investments in any meaningful context to determine significance. RIB at 194-98; RRB at 111-14. Respondents submit that the

[redacted] only appears to relate to the work of a single Microchip employee. RIB at 194-95 (citing Tr. (Smith) at 697:8-25). Respondents argue that the R&D investments that can be allocated to the [redacted] and [redacted] are insignificant in the context of Microchip's overall R&D investments. RIB at 195-97; RRB at 112-13. Respondents further submit that Arigna only relies on [redacted] Microchip employees as part of the asserted domestic industry, which represents a small fraction of Microchip's total headcount. *Id.* at 197-98. Respondents further argue that the investments are not qualitatively significant, with no evidence to corroborate the assertions regarding the importance of [redacted] technology to Microchip or to its position in the marketplace. *Id.* at 198-99. Respondents further submit that there is evidence showing that the technology of the '867 patent is not qualitatively significant, because [redacted]. *Id.* at 199.[77]

Staff submits that Arigna's evidence for significance relates to all [redacted] rather than being limited to the [redacted] and [redacted] SIB at 134. Staff agrees with Respondents that the investments relied upon by Arigna at [redacted] only appear to relate to the work of a single Microchip employee. *Id.* at 135-36; RRB at 58-59. Staff submits that the expenditures identified by Mr. Smith do not represent any significant portion of Microchip's overall operations. SIB at 136-37.

In consideration of the parties' arguments, the undersigned finds that Arigna has failed to show, by a preponderance of the evidence, significant employment of labor or capital with respect to the [redacted] and [redacted] products. As discussed above, Arigna's claimed [redacted] in domestic industry expenditures is an estimate of Microchip's investments for all [redacted]

[77] [redacted] RX-0756C at 3.

products, not the asserted [redacted] and [redacted] products. Arigna has failed to show that the [redacted] in qualifying expenditures allocable to the [redacted] and [redacted] products are significant in any context. These expenditures are a small fraction of Microchip's yearly R&D expenditures of $1 billion. *See* Tr. (Smith) at 699:4-7; CX-00054C. As recognized by Respondents and Staff, the [redacted] identified by Arigna represent a small fraction of Microchip's global workforce of 19,500. *See* JX-00016C (Jaramillo Tr.) at 78:23-79:5. Arigna's assertion that [redacted] also fails to show significance, because the context of this figure is unclear from the record—it relies solely on a few lines of testimony from Mr. Jaramillo regarding [redacted] JX-00016C (Jaramillo Tr.) at 89:2-24. In Mr. Smith's domestic industry analysis, he only [redacted] Tr. (Smith) at 697:20-698:13. Mr. Jaramillo's vague and uncorroborated statement regarding [redacted] is not sufficiently reliable to support a finding of significance. *See Certain Electronic Stud Finders, Metal Detectors and Electrical Scanners*, Inv. No. 337-TA-1221, Comm'n Op. at 54, EDIS Doc. ID 765331, (Mar. 14, 2022) (affirming finding that a single witness's unexplained and unreliable testimony was insufficient to show substantial investments for domestic industry). There is insufficient evidence in the record to determine what the [redacted] testimony is referencing, other than the work of [redacted] Microchip

employee.[78] Arigna has failed to identify, by a preponderance of the evidence, any context in which its domestic industry expenditures are significant.[79]

c. In the Process of Being Established

Arigna submits that the evidence shows a domestic industry in the process of being established based on the R&D work on [redacted] products that is expected to [redacted]. CIB at 233-34; *see* JX-00016C (Jaramillo Tr.) at 256:13-22. Respondents argue that this projection is speculative and even if true, represents a small proportion of the [redacted] that Microchip is currently selling. RIB at 195-97. Staff argues that the sales projection of [redacted] to all [redacted] products and not specifically to the [redacted] or the [redacted] SIB at 138. Staff further argues that the projection is not reliable because Mr. Jaramillo's testimony is uncorroborated by any other evidence. *Id.* at 138-39. Staff submits that Arigna fails to place the sales projection in any meaningful context to assess its significance. *Id.* at 139-40; SRB at 60-61.

In consideration of the parties' arguments, the undersigned finds that Arigna has failed to show, by a preponderance of the evidence, that Microchip has a domestic industry in the process of being established. The Commission has held that a domestic industry is in the process of being established when (1) a complainant takes "the necessary tangible steps to establish such an industry in the United States," and (2) there is a "significant likelihood that the industry requirement will be satisfied in the future." *Certain Stringed Musical Instruments &*

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[78] Mr. Jaramillo referenced this [redacted] in the context of all [redacted] products, JX-00016C (Jaramillo Tr.) at 89:2-24, and accordingly, it would need to be reduced to [redacted] of this figure, or [redacted], in accordance with Mr. Smith's "alternative" allocation.

[79] Because Arigna has failed to show quantitative significance, Arigna's qualitative evidence is irrelevant. *See Lelo Inc. v. Int'l Trade Comm'n*, 786 F.3d 879, 885 (Fed. Cir. 2015) ("Qualitative factors cannot compensate for quantitative data that indicate insignificant investment and employment.").

Components Thereof, Inv. No. 337-TA-586, Comm'n Op. at 13, 2008 WL 2139143, at *8 (May 16, 2008). Moreover, the emergent industry "must prove that it has significant or substantial investments or employment in the United States with respect to articles protected by the patent as recited in the statute." *Certain Non-Volatile Memory Devices and Products Containing the Same*, Inv. No. 337-TA-1046, Comm'n Op. at 41, EDIS Doc. ID 659979 (Oct. 26, 2018). Although Arigna has identified some tangible steps toward establishing a domestic industry with respect to the [redacted] and the [redacted] including [redacted], Arigna has not shown significant investments as of the date of the complaint, as discussed above, and the record does not show a significant likelihood that such investments are forthcoming.

Arigna relies primarily on Mr. Jaramillo's testimony that [redacted]. JX-00016C (Jaramillo Tr.) at 256:13-22. The undersigned agrees with Respondents and Staff, however, that this uncorroborated testimony is unreliable—the Commission has previously found such testimony concerning sales projections to be "unduly speculative." *Certain Thermoplastic-Encapsulated Electric Motors, Components Thereof, and Products and Vehicles Containing Same*, Inv. No. 337-TA-1073, Comm'n Op. at 8, 13-14, EDIS Doc. ID 684974 (Aug. 12, 2019). Moreover, Mr. Jaramillo's testimony only refers to [redacted] products generally, and there is no evidence in the record that indicates which [redacted] (or how many) would incorporate the [redacted] or the [redacted] All of the evidence regarding Microchip's future products is speculative, and on this record, the undersigned cannot find that there is a significant likelihood that Microchip's investments will satisfy the domestic industry requirement in the future.

Accordingly, Arigna has not shown that the economic prong of the domestic industry requirement is satisfied with respect to the ’867 patent.

H. Invalidity

Respondents contend that claims 4 and 8 of the ’867 patent are invalid in view of certain prior art references. RIB at 150-180. In particular, Respondents assert that claim 4 of the ’867 patent is anticipated by International Patent Application Publication WO 2009/060670 to Torii *et al.* (RX-2539, “Torii”). RIB at 150-65. Respondents also assert that claim 8 of the ’867 patent is rendered obvious by U.S. Patent Publication No. 2009/0179261 to Sekiguchi *et al.* (RX-2558, “Sekiguchi”) in view of U.S. Patent Publication No. 2009/0218619 to Hebert *et al.* (RX-2543, “Hebert”). RIB at 165-80.

1. Anticipation of Claim 4

Torii is an international patent application publication with a publication date of May 14, 2009, which is prior art to the ’867 patent. Torii, cover. Respondents contend that Torii anticipates claim 4. RIB at 150-65; RRB at 86-95. Respondents rely on Dr. Bravman’s analysis of Torii’s “Working Example 4” with respect to each limitation of claim 4. Tr. (Bravman) at 839:21-849:25; *see* RX-2549 at ¶¶ 80-93, Fig. 9, Fig. 11. Arigna argues that Torii does not anticipate claim 4, specifically arguing that the claimed “dimension of a part” is critical to the invention and is not disclosed by Torii. CIB at 198-202, 204-210; CRB at 133-35. Arigna also argues that Torii does not disclose the source layer and base layer in contact for the claimed “dimension of a part.” *Id*. at 204-210; RRB at 135-36.

Respondents dispute Arigna’s argument that the range claimed in claim 4 is critical to the invention. RIB at 150-52; RRB at 80-84; *see also* SRB at 35. Staff agrees with Respondents that Torii anticipates claim 4. SIB at 111-14; SRB at 36-45.

The parties' arguments with respect to each limitation of claim 4 are addressed below:

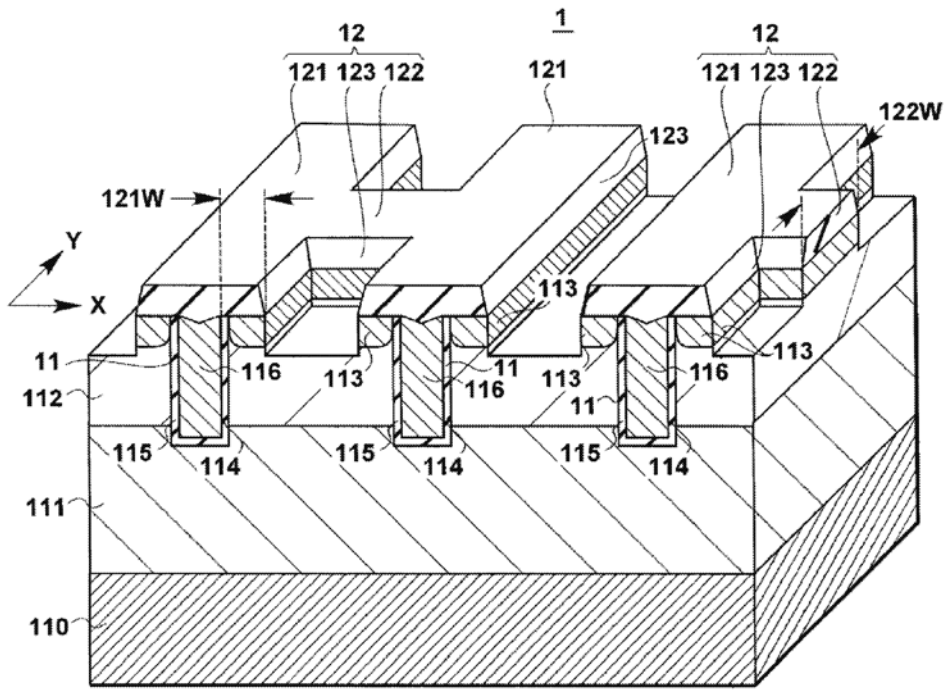
a. "A semiconductor device, comprising"

Torii describes a "semiconductor device and manufacturing method thereof." RX-2539 at Abstract. Specifically, in Working Example 4, "[t]he semiconductor elemnt 1 is the IGBT 11." *Id*. at ¶ 80. There is no dispute that Torii discloses a semiconductor device in accordance with the preamble of claim 4. *See* CIB at 152-53; Tr. (Bravman) at 840:7-10.

b. "a base layer having a first conductivity type"

Torii discloses "a p type second semiconductor region 112 (below called based region 112), which is a p type base region." RX-2539 at ¶ 80. Dr. Bravman identifies the base layer labeled 112 in Figure 9 of Torii. Tr. (Bravman) at 840:11-24; RDX-0003C.108.

FIG. 9



RX-2539.76, Fig. 9. There is no dispute that Torii discloses a base layer having a first conductivity type. *See* CIB at 153.

c. "a source layer formed on said base layer and having a second conductivity type"

Torii discloses "an n type third semiconductor region 113 (below called emitter region 113), which is an emitter region." RX-2539 at ¶ 80. Dr. Bravman identifies the emitter region 113 of Torii formed on the base layer, explaining that the term "emitter" is used to refer to a source layer. Tr. (Bravman) at 841:4-16; RDX-0003C.109. There is no dispute that Torii discloses a source layer formed on the base layer having a second conductivity type. *See* CIB at 145-55.

d. "an insulating film formed on said source layer"

Torii discloses an "interlayer insulation film 12" on the source layer. RX-2539 at ¶ 83; *see* Tr. (Bravman) at 842:14-23. There is no dispute that Torii discloses an insulating film formed on the source layer. *See* CIB at 155.

e. "a plurality of gate structures penetrating said base layer"

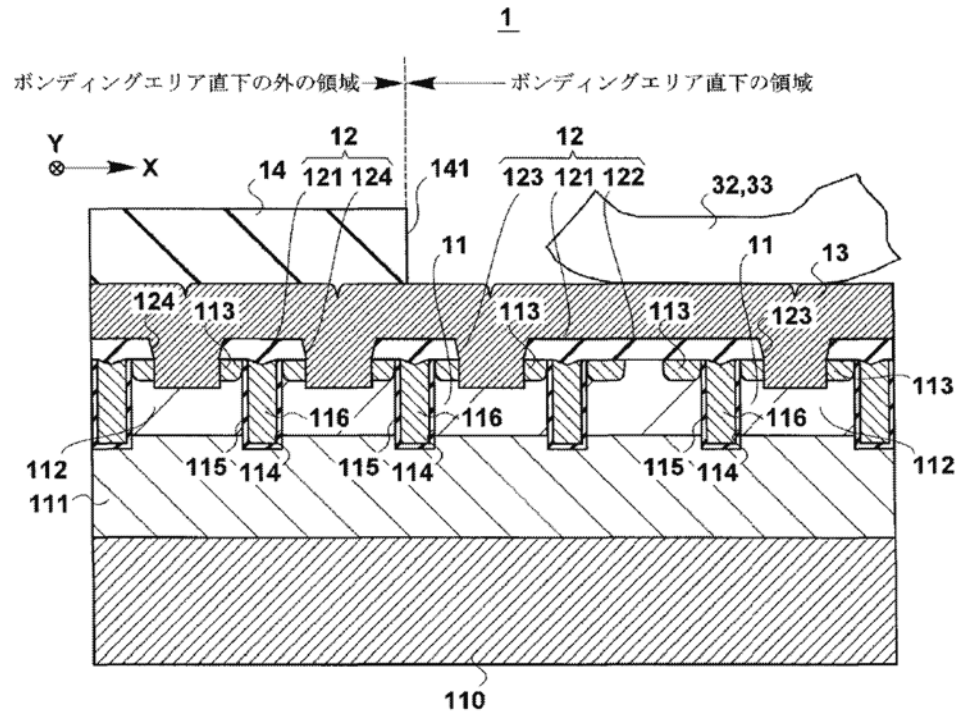
Torii discloses a "gate electrode 116" and "gate insulation film 115" formed in trench 114. RX-2539 at ¶ 80. Dr. Bravman explains that these three structures collectively comprise a "gate structure" penetrating the base layer. Tr. (Bravman) at 842:24-843:19; RDX-0003C.112. There is no dispute that Torii discloses gate structures penetrating the base layer. *See* CIB at 156-57.

f. "a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer"

Torii discloses that "the second electrode (emitter electrode) 13 is provided on the interlayer insulation film 12 and, within the bonding area of the second electrode 13, the second electrode 13 is connected to the IGBT 11 via the aperture 123 of the interlayer insulation film 12." RX-2539 at ¶ 92. Dr. Bravman explains that the apertures in Torii are a plurality of

conductive portions electrically connected to the source layer and base layer, as depicted in Figure 11. Tr. (Bravman) at 843:20-845:3; RDX-0003C.113.

FIG. 11



[upper-left] REGION OUTSIDE OF DIRECTLY BELOW BONDING AREA

[upper-right] REGION DIRECTLY BELOW BONDING AREA

RX-2539, Fig. 11. There is no dispute that Torii discloses conductive portions penetrating the insulating film and source layer and electrically connected to the source layer and base layer. *See* CIB at 157-58.

g. "a source electrode formed on said insulating film and electrically connected to said conductive portions"

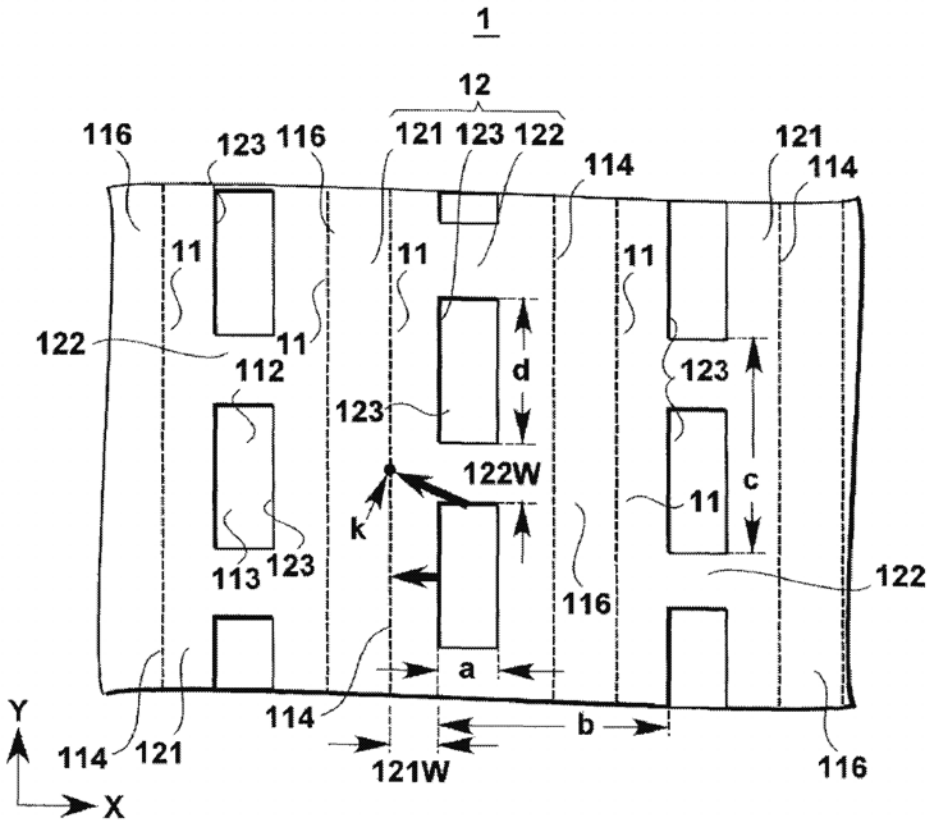
Torii discloses that "the second electrode 13 is connected to the IGBT 11 via the aperture 124 of the interlayer insulation film 12." RX-2539 at ¶ 92. Dr. Bravman explains that this second electrode 13 is the claimed source electrode. Tr. (Bravman) at 845:5-846:2; RDX-

0003C.114. There is no dispute that Torii discloses a source electrode formed on the insulating film and electrically connected to the conductive portions.

h. "said gate structures are formed in a stripe shape in plan view"

Torii discloses in the context of its "Working Example 1" that "hole 114 has a stripe shape." RX-2539 at ¶ 40. In the context of "Working Example 4," these same "holes 114" are shown in Figure 10, and Dr. Bravman explains that this corresponds to the limitation regarding the gate structures shown in plan view. Tr. (Bravman) at 846:4-19; RDX-0003C.115.

FIG. 10



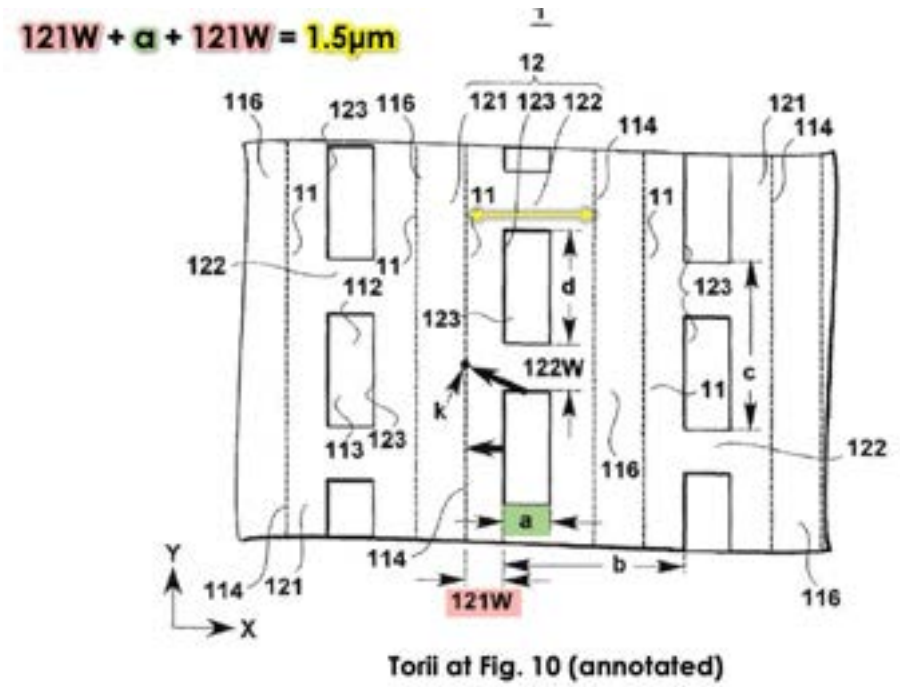
RX-2539, Fig. 10. There is no dispute that Torii discloses gate structures formed in a stripe shape in plan view. *See* CIB at 159-60.

i. "parts in which said conductive portions are connected to said base layer are formed, in plan view, side by side in an island shape in a direction of said stripe shape of said gate structures with a distance from said gate structures between said gate structures"

Torii discloses "apertures 123 arranged in rows at fixed intervals in the first direction and the apertures 123 adjacent on the second direction side therefore are offset." RX-2539 at ¶ 89. Dr. Bravman identifies the apertures 123 shown as "rectangular islands" on Torii's Figures 9 and 10 that are side by side in the direction of the stripe shapes of holes 114. Tr. (Bravman) at 846:21-848:9; RDX-0003C.116. There is no dispute that Torii discloses the island shapes required by this limitation of claim 4. *See* CIB at 160-62.

j. "a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures in a region in which said conductive portions are not connected to said base layer is 0.36 µm or more"

Dr. Bravman identifies disclosures in Torii describing the width "a" of the apertures 123 to be 0.5 µm and the width "121W" of extension parts 112 to also be 0.5 µm. Tr. (Bravman) at 848:10-849:12; RDX-0004C.117-.118 (citing RX-2539 at ¶ 89, Fig. 9, Fig. 10). He explains that the relevant "dimension of a part" requires adding the width "121W" twice to the width "a," which results in a distance between gate structures of 1.5 µm. Tr. (Bravman) at 848:10-849:12.



Torii at Fig. 10 (annotated)

RDX-0003C.118 (citing RX-2539 at ¶ 89, Fig. 10). Dr. Bravman confirmed this width of 1.5 µm by considering Torii's disclosure that the array pitch "b" of the gate structures is 2.0 µm. Tr. (Bravman) at 878:19-879:11, 934:1-935:18; *see* RX-2539 at ¶ 89 ("Array pitch (b) of the holes 114 is 2.0 µm."). Based on Dr. Bravman's analysis of these disclosures in Torii, Respondents thus submit that Torii anticipates the claim limitation requiring the "dimension of a part" to be "0.36 µm or more." RIB at 162-65; RRB at 87-95.

Arigna provided no expert testimony disputing this claim limitation. Based on cross-examination testimony, however, Arigna argues that Torii does not explicitly disclose the relevant dimension of a part and that Dr. Bravman's testimony is insufficient to prove that the dimension is inherently disclosed. CIB at 204-10; CRB at 133-36. Arigna argues that the range "0.36 µm or more" is critical to the operation of the claimed invention, citing case law that precludes a finding of anticipation where the prior art discloses a range that only partially overlaps with the claimed range. CIB at 198-202. Arigna identifies an "ambiguity" in Torii's

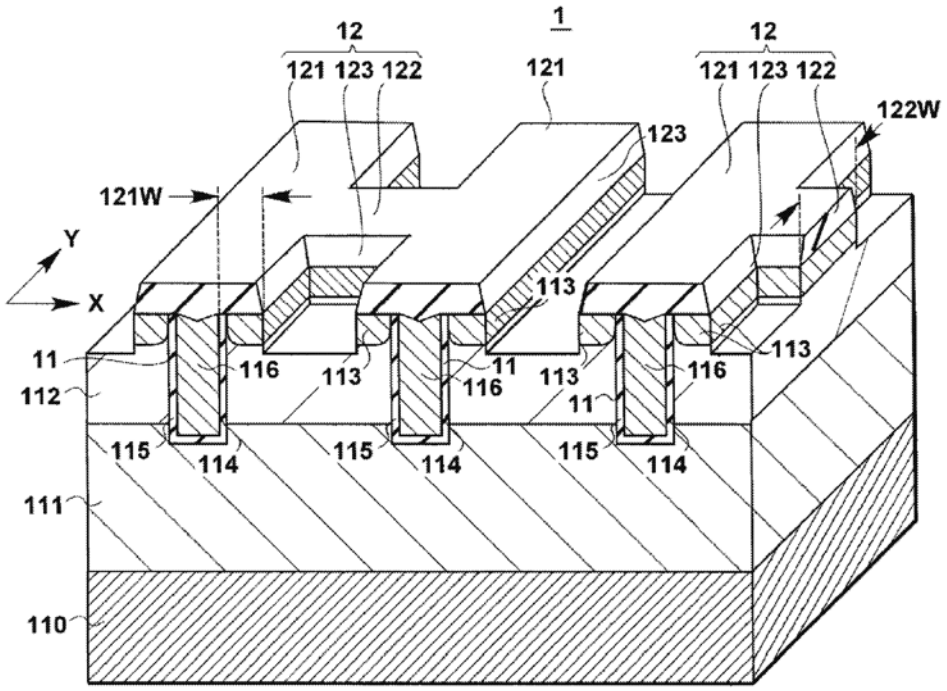
disclosure with respect to the dimension "a," arguing that this precludes a finding of clear and convincing evidence of anticipation. *Id*. at 206-07. Arigna argues that Dr. Bravman's alternative calculation fails to resolve this issue. CRB at 134. Arigna also points to Torii's Figure 11, where the source layer 113 and base layer 112 are not shown to be in contact between the gate structures 116. CIB at 207-08; CRB at 135-36. Arigna argues that Dr. Bravman failed to explicitly address where the source layer and base layer are in contact. CRB at 135. Arigna further argues that Torii's dimension "121W" includes the gate insulation film, which means that it includes part of the gate structure that is not part of the '867 patent's "dimension of a part." CIB at 209-10; CRB at 136.

Respondents and Staff contend that certain of Arigna's arguments regarding anticipation have been waived because they were not raised in Arigna's pre-hearing brief. SIB at 113-14; RRB at 86-87. Staff agrees with Respondents that Torii anticipates the claimed "dimension of a part" under any reasonable interpretation of the measurements disclosed in Torii. SIB at 38-43. Staff further submits that the source layer is shown to be in contact with the base layer in Figure 9 of Torii. *Id*. at 43-44; *see* Tr. (Bravman) at 886:5-888:22. Staff further cites disclosures in Torii showing that the width "121W" does not include the gate insulation film, as argued by Arigna. *Id*. at 44-45 (citing RX-2539 at ¶ 79).

With respect to the arguments regarding waiver, the undersigned agrees with Arigna that the parties are entitled to rely on Dr. Bravman's cross-examination testimony from the hearing, and Arigna will not be precluded from arguing that Respondents failed to carry their burden on invalidity. *See* CRB at 136-38. Even considering Arigna's arguments, however, the undersigned agrees with Respondents and Staff that claim 4 is anticipated by Torii by clear and convincing evidence.

Dr. Bravman clearly showed that the relevant "dimension of a part" disclosed in Torii is 1.5 μm. Tr. (Bravman) at 848:10-849:12; RDX-0003C.117-.118 (citing RX-2539 at ¶ 89, Fig. 9, Fig. 10). Figure 9 of Torii clearly depicts the source layer 113 in contact with the base layer 112 between adjacent gate structures 116.

FIG. 9



RX-2539 at Fig. 9; *see id.* at ¶ 87; RRB at 89. This is a figure that Dr. Bravman relied upon when measuring the relevant "dimension of a part." Tr. (Bravman) at 848:10-849:12; RDX-0003C.117. Arigna argues that Figures 10 and 11 do not show contact between the source layer and base layer where Dr. Bravman measured the relevant dimension, CIB at 207-08, but these other figures show different perspectives that would not be expected to show the relevant contact. *See* Tr. (Bravman) at 886:25-888:25. With respect to Figure 10, Dr. Bravman explains that it is an overhead "plan view," which "can't show the third dimension." *Id*. at 888:2-15. With respect to Figure 11, Dr. Bravman explains that it is a "different cut" through the device.

Id. at 886:25-888:1. Arigna has raised no dispute that the source layer is shown to be in contact with the base layer between gate structures in Figure 9, which is a figure on which Dr. Bravman shows the relevant "dimension of a part." RX-2539 at Fig. 9; *see* Tr. (Bravman) at 848:10-849:12; RDX-0003C.117; Tr. (Bravman) at 888:16-22 (explaining that the distance between gates without a conductive portion is not shown in Figure 11 . . . "[t]hat's why they drew Figure 10 and Figure 9 and other figures."); RRB at 88.

Arigna also identifies a possible ambiguity in Torii where the dimension "a" (in Figure 10) is described as "hole width (a) of the hole ***114***," RX-2539 at ¶ 89 (emphasis added), but the undersigned agrees with Respondents that this is a typographical error, and even if Arigna's interpretation were correct, it does not materially affect Dr. Bravman's analysis of the "dimension of a part." *See* RRB at 89-95. In Figure 10, the label "a" does not indicate the width of the hole 114 but instead indicates the width of an aperture 123. *See* RX-2539 at ¶ 89 and Fig. 10; *see also id*. at ¶ 79 (describing aperture 123 and width 121W in the context of Figures 9 and 10). The dimensions "a," "b," and "d" in Figure 10 are all associated with the aperture 123, not hole 114. *See* RX-2539, Fig. 10. Based on this evidence, the undersigned finds that Torii's reference to the dimension "a" as the width of hole 114 in ¶ 89 is a typographical error, and the width "a" clearly refers to the width of the aperture 123.

Nevertheless, even if the dimensions "a" and "b" set forth in ¶ 89 referred to the width and array pitch of the holes 114, Dr. Bravman explains that the relevant "dimension of a part" would be the same 1.5 μm, based on the array pitch of 2.0 μm and the 0.5 μm width of other parts. *See* Tr. (Bravman) at 934:1-935:18 (citing RX-2539 at ¶ 89); *id.* at 934:11-14, 938:9-11 ("pitch" is the "repeating distance from adjacent elements relative to their center lines or their left edge or their right edge"); *see also* Tr. (Bravman) at 878:13-879:11; RRB at 90-92. This 1.5

μm dimension can be easily obtained by subtracting the 0.5 μm width of hole 114 from the 2.0 μm array pitch. *See* RX-2539 at ¶ 89, Fig. 10; RIB at 91. Accordingly, regardless of how part "a" is interpreted, the evidence shows clearly and convincingly that the "dimension of a part" limitation is met.

The anticipation of this limitation by Torii is also unaffected by Arigna's argument that the width "121W" includes the gate insulation film 115. *See* CIB at 209-10; RRB at 93-95. The calculation of pitch minus hole width 114 does not depend on this issue. *See* RRB at 90-92; RX-2539 at ¶¶ 41-42 ("gate insulation film 115 is arranged along the inner wall and bottom surface of the hole 114"). In addition, Dr. Bravman's testimony that the insulation film width is negligible in the context of measuring the "dimension of a part is corroborated by Figure 10, which labels several widths, including "121W," without identifying the gate insulation film. *See* Tr. (Bravman) at 880:17-881:3 (describing the insulation film width as "a small fraction of the total width of the gate structure"); RX-2539 at Fig. 10. Moreover, because the claim limitation only requires a dimension that is greater than 0.36 μm, the width "121W" is not even necessary to prove anticipation. *See* RRB at 93-95; SRB at 44-45. As discussed above, the width "a" of the aperture part 123 is 0.5 μm, which is already greater than 0.36 μm (and if the "a" and "b" referred to the width and array pitch of the holes 114 under Dr. Bravman's alternative measurement, the "dimension of a part" is 1.5 μm).[80]

[80] As discussed above, this analysis is supported by the expert testimony of Dr. Bravman. Arigna did not object to Dr. Bravman's testimony or move to strike it at the hearing and thus its objections to such testimony (*see* CRB at 134) are waived. In addition, a court is not required to rely on expert testimony regarding a reference's disclosures particularly where, as here, Arigna presented no expert testimony negating anticipation. *See, e.g., Advanced Tech. Materials, Inc. v. Praxair, Inc*., 228 Fed. Appx. 983, 985 (Fed. Cir. Apr. 19, 2007) ("where a prior art reference plainly discloses a claim limitation, the court may recognize and apply that teaching on summary judgment"); *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1329 (Fed. Cir. 2009) ("[i]n many patent cases expert testimony will not be necessary").

With respect to the criticality of the "0.36 μm or more" limitation, the undersigned agrees with Respondents and Staff that the case law regarding criticality is irrelevant to the anticipation arguments with respect to Torii, because Torii does not disclose a range of dimensions that partially overlaps with the claimed range—it only discloses a single dimension of 1.5 μm. *See* RRB at 80-82; SIB at 110; SRB at 35; *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 871 (Fed. Cir. 2015) ("*Ineos*'s criticality evidence is not relevant because that inquiry is appropriate only where the prior art discloses a range, not a particular value within the later claimed range."); *ModernaTx, Inc. v. Arbutus Biopharma Corp*., 18 F. 4th 1352, 1364 (Fed. Cir. 2021) (same). As discussed above, even when considering Arigna's erroneous arguments of ambiguity regarding the precise dimensions disclosed in Torii, the relevant "dimension of a part" cannot be less than 0.5 μm, which would fall within the claimed range. The undersigned thus finds that Torii clearly and convincingly discloses a "dimension of a part" that is greater than 0.36 μm, anticipating this limitation.

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For the reasons discussed above, the undersigned thus finds that claim 4 of the '867 patent is anticipated by Torii.

2. Obviousness of Claim 8

Sekiguchi is a U.S. patent application published on July 16, 2009, which is prior art to the '867 patent. Sekiguchi, cover. Hebert is a U.S. patent application published on September 3, 2009, which is prior art to the '867 patent. Hebert, cover. Respondents contend that Sekiguchi discloses each limitation of claim 8 of the '867 patent except for the claimed range for the "dimension of a part," which is disclosed in Hebert. RIB at 165-80; RRB at 96-97. Respondents submit that it would have been obvious to combine Sekiguchi and Hebert. RIB at 168-70; RRB

at 97-102. Respondents rely on the testimony of Dr. Bravman with respect to Sekiguchi and Hebert. Tr. (Bravman) at 850:2-863:3. Arigna argues that this combination does not render claim 8 obvious, specifically arguing that the claimed "dimension of a part" is critical to the invention and disputing whether one of ordinary skill in the art would have been motivated to combine the references. CIB at 202-04, 210-217; CRB at 138-43. Respondents dispute Arigna's argument that the range claimed in claim 8 is critical to the invention. RIB at 165-68; RRB at 80-81, 84-86; *see also* SIB at 110-11; SRB at 35-36. Staff agrees with Respondents that claim 8 is rendered obvious by Sekiguchi in combination with Hebert. SIB at 114-19; SRB at 46-51.

Each limitation of claim 8 is addressed below:

a. "A semiconductor device, comprising"

Sekiguchi describes "a manufacturing method of a semiconductor device." RX-2558 at Abstract. Dr. Bravman identifies a specific embodiment in Sekiguchi describing a power MOSFET semiconductor device. Tr. (Bravman) at 855:23-856:4; RDX-0003C.125 (citing RX-2558 at ¶ 78). There is no dispute that Sekiguchi discloses a semiconductor device in accordance with the preamble of claim 8. *See* CIB at 170-71.

b. "a base layer having a first conductivity type"

Sekiguchi discloses a "P-base region 23" that includes "P+ body contact regions 31." RX-2558 at ¶¶ 95, 97. Dr. Bravman identifies this region as the claimed "base layer." Tr. (Bravman) at 856:5-17; RDX-0003C.126. There is no dispute that Sekiguchi discloses a base layer having a conductivity type. *See* CIB at 171.

c. "a source layer formed on said base layer and having a second conductivity type"

Sekiguchi discloses "high concentration N+ regions 24 (corresponding to source regions." RX-2558 at ¶ 95. Dr. Bravman explains that these N+ source regions are formed on

the P+ base regions in Sekiguchi. Tr. (Bravman) at 856:18-857:2; RDX-0003C.127. There is no dispute that Sekiguchi discloses a source layer meeting this limitation of claim 8. *See* CIB at 172.

d. "an insulating film formed on said source layer"

Sekiguchi discloses "an interlayer dielectric 5" that "is formed on the main surface 1a of the wafer (the main surface at this time being the upper surface of the high-concentration N+ regions." RX-2558 at ¶ 96. Dr. Bravman explains that this dielectric is an insulating film formed on the source layer. Tr. (Bravman) at 857:4-12; RDX-0003C.128. There is no dispute that Sekiguchi discloses an insulating film formed on the source layer. *See* CIB at 172-73.

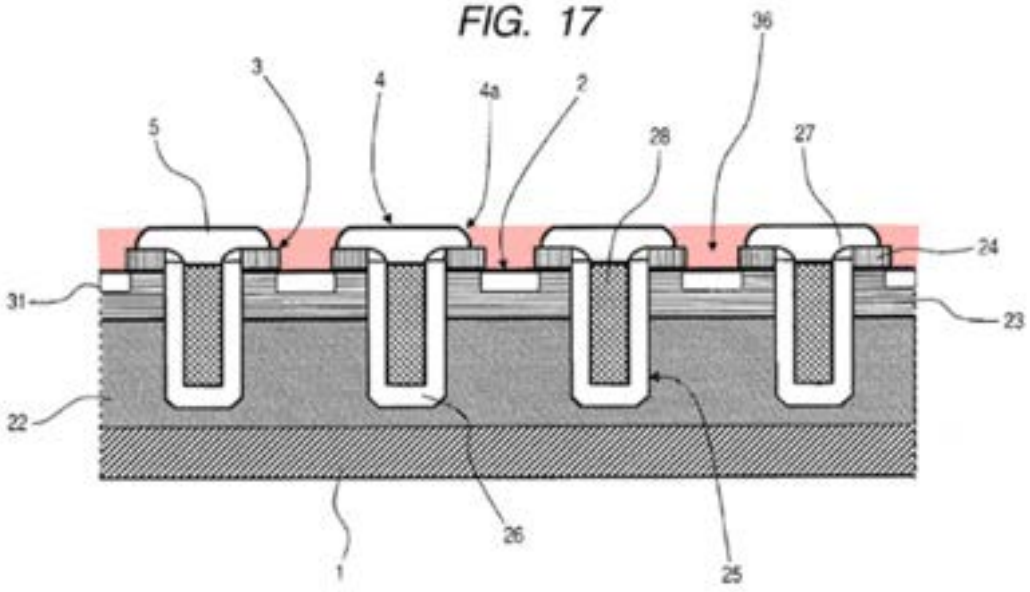
e. "a plurality of gate structures penetrating said base layer"

Sekiguchi discloses "trenches 25" that "are dug in this N-epitaxial layer from its main surface side." RX-2558 at ¶ 95. "Phosphorus-doped polysilicon gate electrodes 28 are embedded into the trenches 25 so as to interpose a gate insulating film 26 therebetween." *Id*. Dr. Bravman explains that this forms gate structures penetrating the base layer. Tr. (Bravman) at 857:14-858:4; RDX-0003C.129. There is no dispute that Sekiguchi discloses a plurality of gate structures penetrating the base layer. *See* CIB at 173-74.

f. "a conductive portion penetrating said insulating film and said source layer, being in contact with an upper surface of said source layer, and electrically connected to said source layer and said base layer"

Sekiguchi discloses "[a] relatively thin barrier metal film 6" and a "relatively thick electrode metal film 7" that are formed within "hole regions 36" that have been etched to expose the source layer and base layer. Tr. (Bravman) at 858:5-849:18; RDX-0003C.130-.132; RX-2558 at ¶¶ 79, 97, 98. Dr. Bravman explains that these two metal films within the openings 36

comprise a conductive portion that penetrates the insulating film and source layer and is in contact with the source layer and connected to the base layer. Tr. (Bravman) at 858:5-860:9.



RX-2558.18, Sekiguchi at Fig. 17 (annotated)

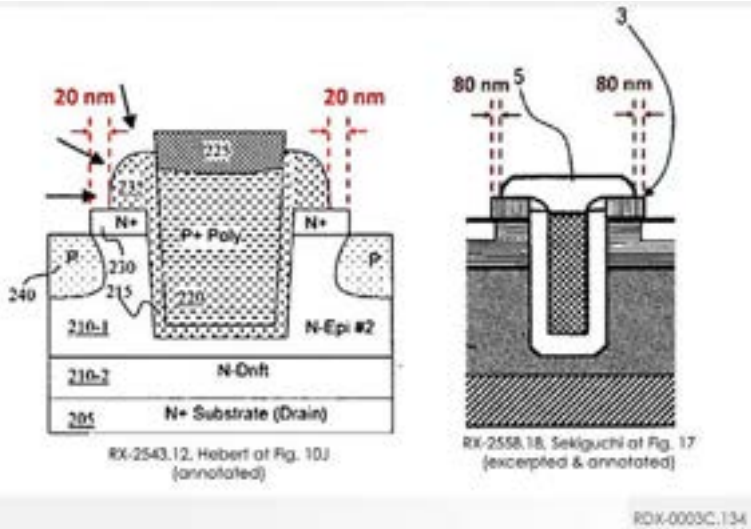
RDX-0003C.132. There is no dispute that Sekiguchi discloses "conductive portions" meeting this limitation of claim 8. *See* RIB at 174-75.

g. "a source electrode formed on said insulating film and electrically connected to said conductive portion"

Dr. Bravman submits that the portions of the barrier metal film 6 and aluminum film 7 that are above the openings 36 correspond to the claimed "source electrode" of the '867 patent. Tr. (Bravman) at 860:10-861:21; RDX-0003C.133. There is no dispute that Sekiguchi thus discloses a source electrode formed on the insulating film and electrically connected to the conductive portion. *See* CIB at 176-77.

h. "wherein a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10nm or more and 40nm or less"

Sekiguchi discloses that the insulating film is "etched off by, for example about 80 nm to form stepwise structures." RX-2558 at ¶ 98. Dr. Bravman identifies a similar process disclosed in Hebert whereby a similar insulating film is etched to a step that is between 20 and 2200nm. Tr. (Bravman) at 861:22-862:20; RDX-0003C.134 (citing RX-2543 at ¶ 38 ("Then a oxide isotropic etch back is performed, e.g., by wet buffer oxide etching (BOE), to reduce the thickness of the space layer 235 of a thickness reduction between 200 Angstroms to 2000 Angstroms to expose the top surface of the source regions 230.")).



RDX-0003C.134. Dr. Bravman explains that the "80 nm" disclosed in Sekiguchi is an "exemplary number" and that "a worker of skill would understand that it was a design decision based on normal experimentation to make tradeoffs between things such as better trench filling and more durable interlayer dielectric layers in the face of the pressures imposed by wire bonding." Tr. (Bravman) at 851:5-852:14. He submits that different widths could be achieved by a "shorter or longer treatment by a buffered oxide etch," which is "just a minor process variation." *Id*. at 852:15-23. He explains that "[t]he rate of etching is well established," and

"[i]t's just a simple matter of time and, perhaps, temperature." *Id*. at 852:24-853:17. He submits that the metallization and etching steps are the same between Sekiguchi and Hebert. *Id*. at 854:3-855:18; RDX-0003C.122-.123. Respondents rely on Dr. Bravman's testimony to argue that the "dimension of a part" limitation is obvious in view of Sekiguchi in combination with Hebert. RIB at 177-79; RRB at 96-101. Staff agrees with Respondents that it would have been obvious for a person of skill in the art to modify the process in Sekiguchi to achieve smaller stairstep structures as disclosed in Hebert. SRB at 48-50.

Arigna argues that the "dimension of a part" limitation of claim 8 is critical to the invention. CIB at 198-204; CRB at 140-42. Arigna argues that this limitation is not rendered obvious by Sekiguchi in view of Hebert because the range of dimensions disclosed in Hebert only partially overlaps with the claimed range. CIB at 211-13; CRB at 138-40. Arigna further argues that the Respondents have failed to prove that a person of ordinary skill in the art would have been motivated to combine Sekiguchi and Hebert. CIB at 213-15; CRB at 142-43; *see* Tr. (Sechen) at 1238:5-1239:1.

In consideration of the parties' arguments, the undersigned finds that Respondents have not met their burden to show, by clear and convincing evidence, that this limitation is obvious in view of Sekiguchi in combination with Hebert.

Respondents argue that Hebert's disclosure of an overlapping range of dimensions establishes a *prima facie* case of obviousness, shifting the burden to Arigna. RIB at 165-66 (citing *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) ("such overlap creates a presumption of obviousness"); *see also In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) ("A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art."). The fact that Hebert

discloses an overlapping range does not relieve Respondents from their burden of proving that one of ordinary skill in the art would have combined Hebert with Sekiguchi, however, because a reason to combine references is part of a *prima facie* case of obviousness. *See Eli Lilly v. Zenith Goldline Pharm.*, 471 F.3d 1369, 1379 (Fed. Cir. 2006) ("[T]o establish a *prima facie* case of obviousness based on a combination of elements in the prior art, the law requires a motivation to select the references and to combine them in the particular claimed manner to reach the claimed invention.").

Respondents submit that modifying the width of the stair-step structure in Sekiguchi would be obvious, because the width is just "a design decision based on normal experimentation to make tradeoffs between things such as better trench filling and more durable interlayer dielectric layers in the face of the pressures imposed by wire bonding." Tr. (Bravman) at 852:7-11. Respondents fail to articulate a reason for reducing the 80nm stair-step structure in Sekiguchi to a width that falls within the claimed range (10-40nm), however. The Federal Circuit has held that "[m]erely stating that a particular placement of an element is a design choice does not make it obvious." *Cutsforth, Inc. v. MotivePower, Inc.*, 636 Fed. Appx. 575, 578 (Fed. Cir. 2016) (quoted in *Polaris Industries, Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 n.4 (Fed. Cir. 2018)).

Respondents rely on Hebert's disclosure of a broad range of dimensions (20-200nm) that overlaps with the claimed range, RX-2543 at ¶ 38, but Respondents do not show that the teaching in Hebert would provide a reason to one of ordinary skill to modify Sekiguchi to achieve a width towards the lower end of that range. *See* RX-2558 at ¶ 98. Sekiguchi discloses a dimension (80 nm) that is in the middle of the range disclosed in Hebert, and it is not clear why Hebert would teach one of ordinary skill to modify the dimension to be significantly smaller

(under 40nm) rather than larger (towards 200nm). Respondents cite *In re Applied Materials, Inc.* to argue that this modification could be made based on routine experimentation, but in that case, the Federal Circuit relied on disclosures in the prior art recognizing that certain claim limitations were "result-effective variables" that could be optimized to achieve desired properties. 692 F.3d 1289, 1295-96 (Fed. Cir. 2012). Respondents identify no such disclosures in Sekiguchi or Hebert, which appear to identify dimensions without disclosing any reasons to vary those dimensions. *See* Tr. (Sechen) at 1238:5-18 (noting that Hebert "does not discuss minimizing or keeping a dimension of a part between 10 and 40 nanometers, or anything close to that in a lateral dimension."); RX-2558 at ¶ 98; RX-2543 at ¶ 38. Dr. Bravman's generic and unsupported testimony that the modification would be "a design decision . . . to make tradeoffs between things such as better trench filling and more durable interlayer dielectric layers in the face of the pressures imposed by wire bonding" is insufficient to show, clearly and convincingly, that one of ordinary skill would have a reason for modifying the 80nm width in Sekiguchi to fall within the range of claim 8. *See* Tr. (Bravman) at 852:7-11; *see also* 862:3-14; *cf. ActiveVideo Networks, Inc. v. Verizon Commn's, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (affirming JMOL regarding obviousness where expert testimony on motivation to combine was "generic . . . and faile[d] to explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*") (emphasis in original); *Microsoft Corp. v. Enfish LLC*, 662 Fed. Appx. 981, 990 (Fed. Cir. Nov. 30, 2016) (affirming PTAB

finding that motivation to combine not shown through declaration asserting that two references "address[ed] the same technical issues and disclose[d] closely related subject matters").[81, 82]

Accordingly, the undersigned finds that Respondents have not shown, by clear and convincing evidence, that the "dimension of a part" limitation of claim 8 of the '867 patent is obvious in view of Sekiguchi in combination with Hebert.

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For the reasons discussed above, the undersigned thus finds that Respondents have not shown, by clear and convincing evidence, that claim 8 of the '867 patent is obvious.

i. Secondary Considerations of Non-Obviousness

Arigna contends that a finding of non-obviousness is further supported by secondary considerations of non-obviousness, including the commercial success of the accused products. CIB at 215-16; CRB at 139-40.[83] The undersigned agrees with Respondents and Staff, however,

[81] Dr. Bravman's testimony is largely directed to identifying similarities between Sekiguchi and Hebert to show that Sekiguchi could be modified with a reasonable expectation of success. *See* Tr. (Bravman) at 850:7-855:22, 898:17-899:5. Arigna also disagrees with this assertion, arguing that if the Sekiguchi process were applied to Hebert, the relevant structure would be etched off completely. CIB at 213-14. Regardless of this issue, what the record lacks is a reason to make such a modification that would result in a dimension within the claimed range.

[82] The parties also dispute whether the claimed 10-40nm range is "critical" to the alleged invention. *See* CIB at 198-200, 202-04; CRB at 140-42; RIB at 165-68; RRB at 84-86; SIB at 110-11; SRB at 35-36. This undersigned does not reach this issue because Respondents have failed to make a *prima facie* case for obviousness. *See E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) (recognizing that a patentee can rebut a *prima facie* case of obviousness by showing that a claimed range is "critical").

[83] Arigna also alleges that there is evidence of long-felt need and failure of others, CIB at 216-17, but the undersigned agrees with Respondents that these arguments have been waived because they were not raised in Arigna' pre-hearing brief. *See* RRB at 102 n.19; CPHB at 11-13. Even if these contentions had been timely raised, the undersigned agrees with Respondents and Staff, RRB at 101-02, SRB at 50-51, that there is no evidence in the record of any stated need for the structure of claim 8 of the '867 patent or any evidence that others attempted to make structures with the claimed dimensions but failed. *See Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004) ("Absent a showing of long-

that the record fails to show commercial success with respect to claim 8 of the '867 patent, because there is no evidence of a nexus between the commercial success of accused vehicles and the '867 patent. *See* RIB at 179; SRB at 50. As discussed above in the context of infringement, the record does not show that any accused vehicle contains a chip that infringes this claim, which precludes any finding of nexus. Moreover, as discussed above in the context of the '082 patent, Arigna provides no context for the sales volume, and both parties' economic experts agreed that the accused vehicles represent a very small share of the hybrid and electric vehicle market. *See* Tr. (Smith) at 652:19-659:2; CDX-003C.3-11; Tr. (Graham) at 1002:11-13. In addition, the record does not show that the sales of any vehicles were due to the width of the stair-step structure of the contact trench in a chip that is part of an inverter or charge regulator, rather than other features of these vehicles. *See Ormco Corp. v. Align Tech., Inc.,* 463 F.3d 1299, 1312 (Fed. Cir. 2006) ("[I]f the commercial success is due to an unclaimed feature of the device, the commercial success is irrelevant."). Accordingly, the undersigned finds that the alleged commercial success of the accused vehicles does not indicate non-obviousness of claim 8.

VI. CONCLUSIONS OF LAW

Based on the foregoing, and the record as a whole, it is the undersigned's final initial determination that there has been no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, and/or the sale within the United States after importation of certain power inverters and converters used in automobiles, components thereof, and automobiles containing those power inverters or converters by reason of infringement of claims of the '082 patent or the '867 patent.

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felt need or the failure of others, the mere passage of time without the claimed invention is not evidence of nonobviousness.").

This determination is based on the following conclusions of law:

1. The Commission has subject matter jurisdiction over this investigation and *in personam* jurisdiction over Respondents.

2. Certain accused products have been imported into the United States, sold for importation, and/or sold within the United States after importation.

3. The Commission has *in rem* jurisdiction over certain accused products.

4. The accused products do not infringe claims 1, 13, 17, or 29 of the ’082 patent.

5. The technical prong of the domestic industry requirement has been satisfied with respect to claims 1, 13, 17, and 29 of the ’082 patent.

6. The economic prong of the domestic industry requirement has been satisfied with respect to the ’082 patent.

7. Claims 1, 13, 17, and 29 of the ’082 patent are invalid.

8. The accused products do not infringe claim 8 of the ’867 patent.

9. The technical prong of the domestic industry requirement has been satisfied with respect to claim 4 of the ’867 patent.

10. The economic prong of the domestic industry requirement has not been satisfied with respect to the ’867 patent.

11. Claim 4 of the ’867 patent is invalid.

The undersigned hereby certifies the record in this investigation to the Commission with the undersigned’s final initial determination. Pursuant to Commission Rule 210.38, the record further comprises the Complaint and exhibits thereto filed with the Secretary, and the exhibits attached to the parties’ summary determination motions and the responses thereto. 19 C.F.R. § 210.38(a).

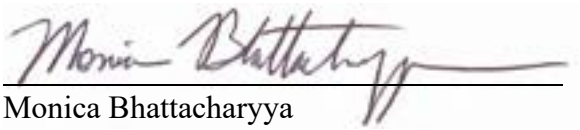
Pursuant to Commission Rule 210.42(c), this initial determination shall become the determination of the Commission 45 days after the service thereof, unless a party files a petition for review pursuant to Commission Rule 210.43(a), the Commission orders its own review pursuant to Commission Rule 210.44, or the Commission changes the effective date of the initial

determination. 19 C.F.R. § 210.42(h)(6).

This initial determination is being issued with a confidential designation pursuant to Commission Rule 210.5 and the protective order in this investigation. Within 10 days of the date of this document, the parties shall submit a joint statement as to whether or not they seek to have any portion of this document deleted from the public version. If the parties do seek to have portions of this document deleted from the public version, they must submit a single proposed public version of this final initial determination with any proposed redactions consistent with the manner specified by Ground Rule 1.9. The submission shall be made by email to Bhattacharyya337@usitc.gov and need not be filed with the Commission Secretary.

Redactions should be limited to avoid obscuring the reasoning underlying the decision. Parties who submit excessive redactions may be required to provide an additional written statement, supported by declarations from individuals with personal knowledge, explaining why each proposed redaction meets the definition for confidential business information in 19 C.F.R. § 201.6(a).

SO ORDERED.



Monica Bhattacharyya
Administrative Law Judge